PUBLIC VERSION

UNITED STATES INTERNATIONAL TRADE COMMISSION

Washington, D.C.

In the Matter of	)	
	)	
CERTAIN VIDEO GRAPHICS DISPLAY CONTROLLERS AND PRODUCTS CONTAINING SAME	)	Investigation No. 337-TA-412
	)	
	)	
	)	

Initial Determination

Appearances:

Michael A. Jacobs, G. Brian Busey, Grant L. Kim, David M. Levin, Russell B. Hill, Harold J. McElhinny, Zachariah A. Higgins, Dana S. Baker, Bryan A. Schwartz and Seth E. Brown of Morrison and Foerster, LLP on behalf of Complainant, Cirrus Logic, Inc.

Ruffin B. Cordell, Ralph A. Mittelberger, Linda Liu Kordziel, Michael J. McKeon, Brian R. Nester, James Pooley, John W. Thornburgh and Wayne Willenberg of Fish and Richardson P. C. on behalf of Respondent, ATI Technologies Inc.

Thomas S. Fusco, Jeffrey R. Whieldon, and Lynn I. Levine on behalf of the Office of Unfair Import Investigations, U. S. International Trade Commission

Debra Morriss, Presiding Administrative Law Judge:

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Procedural Background

On July 1, 1998, Cirrus Logic, Inc. ("Cirrus"), a California corporation, filed a complaint under 19 U.S.C. § 1337 ("Section 337") based on the alleged importation into the United States, the sale for importation, and the sale within the United States after importation of certain video graphics display controllers and products containing same[1] by the proposed respondent, ATI Technologies Inc. ("ATI"), a Canadian corporation. The Commission issued its notice of investigation on July 28, 1998, instituting this Section 337 investigation concerning Cirrus' allegations of ATI's infringement of claims 37 and 43 of United States Patent No. 5,598,525 ("the '525 Patent") owned by Cirrus, as well as Cirrus' claim of the requisite domestic industry. The Commission named Cirrus as the Complainant, and ATI as the sole Respondent in this investigation.

By Order No. 3, issued August 21, 1998, a target date of August 2, 1999 for completion of this investigation was established. All parties made appearances at a preliminary conference on September 16, 1998, at which a procedural schedule was set. On October 14, 1998, Cirrus filed a motion to expand the investigation to include allegations of ATI's

[1]The technology at issue in this investigation concerns devices that manage the computer display of graphics and video, including the display of graphics over video on a graphics background. Graphics data is represented in a red, green and blue ("RGB") format, while video data is represented in a luminance-chrominance ("YUV") format, and these different formats contribute to the design challenges associated with video graphics display controllers. These controllers regulate the storage, scaling, and display of graphics and video data.

infringement of claims 1-10, 12-21, 23-24, 37 and 43 of the '525 Patent. This motion was granted by an initial determination issued on October 29, 1998, which the Commission on November 25, 1998 determined not to review. On January 20, 1999, Cirrus filed a notice withdrawing its infringement allegations as to certain claims and representing the parties' agreement that only claims 13, 15, 16, 17, 23 and 37 remain in dispute. Accordingly, the notice of investigation in this matter is hereby amended to include only claims 13, 15, 16, 17, 23 and 37 of the '525 Patent. ATI's accused products are the Rage Pro, Rage Pro LT and Rage 128. Cirrus requests relief in the form of a permanent exclusion order and a permanent cease-and-desist order.

By motion filed November 25, 1998, ATI moved for summary determination as to the invalidity of claims 37 and 43 of the '525 Patent, which motion was denied by Order No. 38. On December 11, 1998, Cirrus moved for summary determination as to its satisfaction of the economic prong of the domestic industry requirement, which motion was denied by Order No. 45.

The hearing in this matter commenced on January 21, 1999, and concluded on January 29, 1999. All parties were represented at the hearing, as well as at a tutorial conference held January 7, 1999. Subsequent to the hearing, initial and reply briefs, as well as proposed initial and reply Findings of Facts and Conclusions of Law and comments to the initial Findings and Conclusions were filed by the parties. These submissions have been fully considered in reaching this decision and any omission of a discussion of an issue raised by the parties or of a portion of the record does not indicate that it has not been considered. Rather, such issues and/or portions of the record were found to be irrelevant, immaterial and/or without merit.

Additionally, any objections which may not have been ruled on to date and which may remain outstanding are hereby denied.

On April 27, 1999, Cirrus filed a Notification with an accompanying Declaration stating that Cirrus recently located hundreds of pages of documents responsive to pre-hearing discovery requests by ATI. These documents were covered by previous orders to compel in this investigation, and Cirrus was previously sanctioned by entry of a rebuttable adverse factual inference, in Order No. 47, for its repeated deficiency in searching for and producing the same category of documents that are the subject of Cirrus' latest untimely production. Because this category of documents relates to ATI's Section 102(a) "on-sale bar" defense concerning Cirrus' Nordic 7542 product, Cirrus, in its Notification, agrees to "... stipulate conclusively, for purposes of this investigation, that Nordic 7542 was on-sale before the bar date." Cirrus Notification at 4. Although Cirrus also represents in its Notification that it would agree to an extension of the target date and deferral of the initial determination for purposes of additional discovery and possibly submissions related to these documents, no party requested such a deferral or extension. Accordingly, in light of the untimely production of documents in violation of earlier orders to compel, it is a conclusively established finding of fact that Cirrus offered the Nordic 7542 product for sale in the United States before January 23, 1994.

I. Jurisdiction

A. Importation

Section 337 requires an "importation" or a "sale for importation" as a condition of the Commission's exercise of jurisdiction over any accused goods. Enercon GmbH v. Int'l Trade

Comm'n, 151 F.3d 1376 (Fed. Cir. 1998). ATI does not dispute that it imports into the United States the accused products, the Rage Pro, Rage Pro LT and Rage 128 (collectively, "Rage Devices" or "Rage Products"). This stipulation therefore satisfies the importation requirement in Section 337.

B. Domestic Industry

As a prerequisite to reliance on Section 337(a)(1)(B), Cirrus must establish that "...an industry in the United States, relating to the articles protected by the patent ... concerned, exists or is in the process of being established." 19 U.S.C. § 1337(a)(3). Typically, the domestic industry requirement of Section 337 is interpreted as consisting of two prongs: economic and technical. E.g., Certain Variable Speed Wind Turbines and Components Thereof, Inv. No. 337-TA-376, Comm'n Opinion at 14-17 (1996). The economic prong concerns the investment in a domestic industry, while the technical prong involves whether the claimed investment pertains to material protected by the patent. The domestic industry for articles protected by the '525 Patent must involve: (1) significant investment in plant and equipment; (2) significant employment of labor or capital; or (3) substantial investment in its exploitation, including engineering, research and development, or licensing. 19 U.S.C. § 1337(a)(3). Proof of meeting any one of these three criteria satisfies a complainant's burden of proof on the domestic industry requirement. Certain Concealed Cabinet Hinges and Mounting Plates, Inv. No. 337-TA-289, Comm'n Opinion at 19-20, 22 (1990). To make its

domestic industry showing, Cirrus relies on its CL-GD5465 product.[2]

The parties take divergent positions regarding the appropriate point in time from which to analyze domestic industry. Cirrus relies on Bally/Midway Mfg. Co. v. U.S. Int'l Trade Comm'n, 714 F.2d 1117 (Fed Cir. 1983) in support of its contention that the determination must be made as of the date the complaint was filed. ATI, on the other hand, argues that the analysis should be made as of the time of the hearing. This dispute stems from Cirrus' announcement in September 1998 that it intended to phase out its graphics business, and ATI's contention that as a result, by the time of the hearing, Cirrus lacked the requisite domestic industry. Cirrus responds that even using, *arguendo*, the date proposed by ATI, a domestic industry still exists based on ongoing sales and ongoing expenditures for research and development. The Staff contends that Cirrus' phase-out announcement does not preclude its satisfaction of the domestic industry requirement, citing Variable Speed Wind Turbines and Components Thereof, Inv. No. 337-TA-376, Comm'n Opinion at 18 (1996) and Battery-Powered Ride-On Toy Vehicles, Inv. No. 337-TA-314, Comm'n Opinion (1991) and Initial Determination on Motion for Summary Determination (1990), in support thereof.

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[2]Although Cirrus also makes reference to its 5446 product in its post-hearing submissions, ATI and the Staff correctly contend that Cirrus is precluded from relying on this product to establish the requisite domestic industry. Cirrus' omission in its pre-hearing brief of any discussion of this product as a basis for domestic industry, other than its statement in footnote 2, at 8, that it " ... will if necessary demonstrate that the GL-GD 5440, 5446, and 5480 practice representative claims of the patent", is fatal to its subsequent attempt to rely on the 5446. See Ground Rule 7 ("Any contentions not set forth in detail [in the prehearing brief] as required herein shall be deemed abandoned or withdrawn....."). Cirrus' prehearing brief indicated reliance on the 5465 product to prove domestic industry.

1. Economic Prong

Cirrus contends that it satisfies the economic prong, and that it actually meets all three of the criteria set forth above. Cirrus points to its United States manufacturing joint venture with IBM, MiCRUS, as evidence of its substantial investment in exploiting the '525 Patent, citing multimillion dollar investments in the MiCRUS plant and equipment. MiCRUS, which operates a semi conductor wafer manufacturing facility in East Fishkill, New York, has served as the fabrication facility for all the 5465 products sold by Cirrus, and, although it is not currently manufacturing additional 5465 products, Cirrus continues to accept orders for existing inventory. Cirrus further claims that its investment in research and development associated with the '525 Patent independently satisfies the economic prong, as the research for and development of the 5465 product occurred in the United States, and as it continues to make payments under a contract with ISD Corporation for research and development related to the 5465 product. Cirrus also maintains that its licensing activities serve as a basis for finding a domestic industry, as it has licensed the '525 Patent to [

] and as it continues to seek other licensors for the '525 Patent.

ATI disputes Cirrus' establishment of the economic prong of domestic industry, instead maintaining that as of the hearing date, Cirrus lacked a sufficient domestic industry. ATI asserts that since at least June 1998, Cirrus has not manufactured the 5465 product, and that Cirrus failed to show sales of the 5465 product from November 1998 to the time of trial. As to investment in labor, ATI states that as of at least January 1999, Cirrus no longer employs any research and development personnel and Cirrus has eliminated its graphics division. ATI claims that Cirrus has not met its burden of proof to establish that any of the work performed

by ISD Corporation relates to the 5465 product. ATI next contends that Cirrus' licenses with [ ] cannot serve as the basis for satisfying domestic industry absent any showing that [ ] actually practices the '525 Patent, and, as to [ ] license, ATI claims a lack of evidence that [ ] from Cirrus even includes the '525 Patent. ATI also notes that these licenses are [ ] such that the '525 Patent is "tangential and insignificant", and Cirrus failed to allocate any portion of the license payments to the '525 Patent.

The Staff analogizes the facts relevant to the economic prong in this investigation with those in the Wind Turbines and Toy Vehicles investigations, and concludes that the findings of satisfaction of the economic prong in those cases warrant such a finding here. The Staff stresses that Cirrus has not ceased all activity relating to the 5465 product, even though Cirrus no longer manufactures it.

Commission precedent supports a finding that Cirrus satisfies the economic prong in this investigation. In Toy Vehicles, the Commission adopted a portion of the Initial Determination, including a finding of domestic industry, despite the patentee's having halted manufacture of the product covered by the patent in order to manufacture a new and improved model. See Initial Determination at 19-20. The domestic industry proof in that case rested heavily on the patentee's prior investment in facilities, labor, equipment and research to obtain the patent and develop a product that practiced it, or alternatively on the continued sale of existing inventory of the covered product as replacement parts, even where this ongoing sale failed to generate significant revenue. Id. at 20-21. In Wind Turbines, the Commission upheld a domestic industry finding even where the patentee had filed for bankruptcy and had recently

ceased manufacturing the device covered by the patent at issue, noting the complainant's past investment in the various categories set forth in Section 337(a), and its continued exploitation of the patent, albeit in a more limited fashion. Comm'n Opinion at 17-18. The 1988 amendment to the domestic industry statutory language of Section 337 and its legislative history support a liberal and flexible interpretation of the requirement. See H.R. Rep. No. 100-40, 100th Congress, 1st Sess. (1987); Wind Turbines, Comm'n Opinion at 17 ("...[T]he domestic industry determination is not made by application of a rigid formula...").

Cirrus' showing for the economic prong of domestic industry appears at least as strong as the complainants' showings in Toy Vehicles and Wind Turbines. That Cirrus is not currently manufacturing the 5465 product is not dispositive, as the evidence shows that Cirrus has invested substantial capital in developing and manufacturing the 5465 product, and uncontradicted testimony establishes that Cirrus is currently offering for sale and intends to continue offering for sale an existing inventory of the product. Additionally, the evidence is undisputed that, in exchange for a significant monetary payment, Cirrus has licensed the '525 Patent to at least one third party. Credible evidence of record also shows that Cirrus is paying ISD Corporation for research and development activities, including continuation of software development and maintenance for the 5465 product. The sum total of Cirrus' past as well as present investment associated with the 5465 product, coupled with Cirrus' activity related to licensing the '525 Patent support a finding of domestic industry at any point from the time of the filing of the complaint through the date of the hearing.

2. Technical Prong

Cirrus bears the burden of proving that its domestic industry practices a valid claim of

the '525 Patent. See Certain Removable Electronic Cards and Electronic Card Reader Devices and Products Containing Same, Inv. No. 337-TA-396, Comm'n Opinion at 2, 17 (1998); Certain Variable Speed Wind Turbines and Components Thereof, Inv. No. 337-TA-376, Comm'n Opinion at 14, 17 (1996); Certain Microsphere Adhesives, Process for Making Same, and Products Containing Same, Including Self-Stick Repositionable Notes, Inv. No. 337-TA-366, Comm'n Opinion at 7-8, 13-14 (1996); 19 U.S.C. § 1337(a). Cirrus argues that it satisfies the technical prong as the 5465 practices Claim 13 by meeting each of the limitations of that claim,[3] while ATI contends that Cirrus has not demonstrated that each and every element of Claim 13 appears in the 5465 product, and that in any event, the claim is invalid. The Staff asserts that the technical prong is not met as the 5465, in its view, does not satisfy the "when" condition of Claim 13.

For the reasons set forth under the claim construction section *infra*, I have concluded that the "when" condition is invalid for indefiniteness and that Claim 13 is therefore not a valid claim. Additionally, even if it were a valid claim, I have determined, after considering below the other elements of that claim, that the "frame buffer" element and the "first port" limitation are missing from the 5465 product, such that it may not be found to practice the claim irrespective of the "when" condition. Accordingly, I find that Cirrus has not satisfied its

[3]I note that Cirrus, in its Prehearing Brief, argued only that it would "demonstrate that each limitation of representative claims 1, 2, 3, 6 and 37 are found in the GL-GD 5465", Cirrus Prehearing Brief at 8, and made no mention of Claim 13. Because neither ATI nor the Staff objected in post-hearing submissions, however, to the omission from the Prehearing Brief of an analysis or argument as to Claim 13, the objections were waived. See Ground Rule 20 ("It is counsel's responsibility to make the Administrative Law Judge aware of infractions by making a timely objection. Failure to make a timely objection will result in the conclusion that counsel consents to a waiver of the Rule.")

burden with respect to the technical prong of the domestic industry requirement of Section 337.

As indicated in the discussion of the 5465 below, ATI repeatedly criticizes Cirrus' assertions about the 5465's alleged practice of Claim 13 of the '525 Patent where Cirrus offers CX 61C, CX 62C and Mr. Richard Ferraro's testimony as its support. ATI maintains that, in giving his opinions on the 5465, Cirrus' expert, Mr. Ferraro, relied on CX 61C and CX 62C, which ATI contends are marketing documents of such high level that they lack sufficient detail to show the features as to which Mr. Ferraro opined. I note here, as a threshold matter, that for the most part, to the extent this constitutes ATI's *sole* argument against the satisfaction of a claim limitation by the 5465, ATI's argument is rejected. Mr. Ferraro indicated that in connection with forming his expert opinions, he reviewed, *inter alia*, the CL GD 5465 Preliminary Data Book, Version 2.0, the CL GD 5465 Visual Media 3D Graphics Accelerator Data Sheet, the CL GD 5465 Preliminary Product Bulletin, the CL GD 5465 Technical Reference Manual, the Laguna 3DA specification, the deposition transcripts of Mr. John Schafer and the deposition transcript of Mr. Robert Nally. See CX 745C at 3. Thus, while Mr. Ferraro may have noted on a claim chart or cited CX 61C and/or CX 62C to support his opinions on certain claim elements being met in the 5465 product, these documents apparently did not serve as his exclusive source of information about the product manufactured by Cirrus, the party by whom he was retained as an expert in this investigation. Accordingly, where ATI cites no contradictory evidence about the features or functionality of the 5465, and disputes Cirrus' assertions only based on this argument relating to CX 61C and CX 62C, I deem ATI's position unpersuasive.

Turning to the first element, Cirrus alleges that the 5465 is a controller inasmuch as it

is a single video and graphics display controller implemented on a single integrated circuit, representing an integrated design. Although, for the reasons discussed *infra*, I have rejected Cirrus' proposed construction of "a controller" as being limited to a unitary integrated design, the adopted construction nonetheless includes such a design. I therefore find that the 5465 satisfies that element of Claim 13. In reaching this determination, I have considered that ATI, in its response to Cirrus' Proposed Findings of Fact, states that the evidence Cirrus cites, CX 261C, in support of its proposed finding that the 5465 is a core VGA controller with video playback acceleration and video capture features, relates to the 5446 product, not the 5465. While Cirrus, as support for its proposed finding, did in fact incorrectly cite to the functional specifications for the 5446, the record otherwise supports the fact that the 5465 includes "a controller" within the meaning of Claim 13. See CX 61C and CX 62C. Additionally, I note that ATI did not advance in its Post-Hearing Brief or Reply Brief any arguments asserting that the 5465 is not a controller.

Cirrus next contends that the 5465 contains Claim 13's required "circuitry for writing selectively each received word of data into [a] selected one of on-screen and off-screen memory spaces of a frame buffer". Specifically, Cirrus states that the 5465 includes a memory controller which writes graphics and video pixel data into a frame buffer which is divided into on-screen and off-screen areas and that the data is selectively written into those areas. In order to determine whether the 5465 practices this claim element it is necessary to consider whether the 5465 meets both the "circuitry for writing selectively " and "frame buffer" limitations of this claim. The "circuitry for writing selectively" portion of this claim element, as construed *infra*, means that the circuitry, in writing data into memory, can select between the on-screen

region and the off-screen region, as appropriate, according to the address of the word of data. Cirrus relies on CX 61C at CL88354, CX 62C at CL89104-5 and CX 745C at 99-101 (Ferraro Supplemental Report) as evidence that the memory controller of the 5465 writes graphics pixel data into the on-screen space of the frame buffer and video data into the off-screen space of the frame buffer. As referenced in the introductory portion of this section, ATI contests the sufficiency of CX 61C and CX 62C and Mr. Ferraro's reliance on them. For the reasons set forth above, this argument is rejected. Additionally, I note that Mr. John Schafer, who participated in the development of the 5465, testified that the 5465 memory controller utilizes address data to determine where in the frame buffer the data is written. Schafer, Tr. at 581, 584. I find therefore that the record is sufficient to establish that the 5465 has "circuitry for selectively writing" within the meaning of this portion of the claim element.

As to the "frame buffer" limitation of this claim element, I have first considered ATI's contention that the 5465 fails to satisfy this element of Claim 13 of the '525 Patent as it cannot store YUV video data and RGB graphics data in both the on-screen and off-screen areas of the frame buffer as required by Claim 13, but instead stores YUV video data in only the off-screen area. In response, Cirrus alleges that ATI's argument depends on an incorrect claim construction of the term "frame buffer," and that the proper construction does not require YUV data to be stored in the on-screen region.

In construing the "frame buffer" limitation of Claim 13, I have concluded, *infra,* that the claim language and specification support the conclusion that the frame buffer must be able to store graphics or video data in each region. Cirrus does not take issue with ATI's factual statement that the 5465 stores YUV data in only the off-screen area of the frame buffer, and

concedes, in CFF 89, that CX 62C shows that the 5465's frame buffer stores graphics in the on-screen region and video in the off-screen region. I therefore concur with ATI's contention that the 5465 product does not meet the "frame buffer" limitation because each of its memory areas does not have the ability to store either type of data.

Cirrus further contends that the 5465 contains the "first port" element of Claim 13 as it has a host bus interface that accepts pixel data from a host computer, all pixel data received is associated with an address which determines where the data is written into memory, and the address accompanying the data through the host port provides that data written into on-screen memory is treated as graphics and data written into off-screen memory is treated as video. ATI in response argues that certain evidence relied upon by Cirrus, namely Mr. Schafer's testimony, Mr. Ferraro's Supplemental Report (CX 745C at 99-101), and the 5465 Technical Reference Manual, CX 62C at CL88432, does not show that the addresses accompanying the data through the host port of the 5465 determine where in the frame buffer that data is stored or how the data is treated in the backend pipelines.

In construing this element of Claim 13 *infra*, I have determined that the first port element requires that the first port decode the received address, and use it to direct further processing of the data as graphics or video. Based upon my review of the record, I find that the evidence, particularly the testimony from Mr. Schafer, Tr. at 583-84, indicates that in the 5465, the address only directs where the data should be written in the frame buffer memory, and the interface receiving the data with accompanying addresses does not perform frontend processing using the addresses to identify data as graphics or video. Although data deposited in the on-screen area of memory is processed as graphics, whereas data deposited in the off-

screen area is *typically* processed as video, this alone does not meet the "first port" limitation of Claim 13. See Schafer, Tr. at 583-85; CX 63C at CL 87991. In this regard, I note that while the separate memory areas for graphics and video in the 5465 may render frontend processing unnecessary, such frontend processing is nonetheless required by the '525 Patent. Accordingly, I conclude that the 5465 fails to meet this element of Claim 13.

Cirrus next maintains that the 5465 meets the "second port" and "circuitry for generating an address" elements of Claim 13. As set forth in the claim construction section, *infra*, these limitations require an external interface that receives data from a real-time video source and, because the real-time video data lacks an address, circuitry to generate an address so that the data can be written into the frame buffer.

With respect to the "second port" element of Claim 13, Cirrus claims this is satisfied as the 5465 has a V-Port for receiving real-time video which is accepted from an external decoder. Cirrus also contends that the 5465 has address-generating circuitry to create addresses for the real-time video data. Cirrus asserts that this circuitry utilizes video framing signals and other parameters to generate addresses for the real-time video data which are then provided along with the video data to the memory controller and that the memory controller then writes the video data to the frame buffer memory.

Cirrus, as support for its contentions, relies on Mr. Schafer's testimony, (Schafer, Tr. at 587-89), Mr. Ferraro's Supplemental Report, (CX 745C at 99-101) and CX 62C. While ATI raises no challenge to Cirrus' assertion that the 5465 has a V-Port for receiving real-time video data, ATI, in response to Cirrus' Proposed Findings of Fact concerning the "circuitry for generating an address" limitation, contests the sufficiency of CX 62C as well as Mr. Ferraro's

opinion. For the reasons set forth above, this argument is rejected, as ATI cites to no evidence contradicting Mr. Ferraro's opinion. Additionally, I note that Mr. Schafer testified that the 5465 has a video interface that provides a means to connect to a real-time video source, that in the 5465 addresses are generated for the real-time video that comes in through the video port, and that these addresses are provided to the memory controller. Schafer, Tr. at 587-88. I therefore find that the 5465 satisfies the "second port" and "circuitry for generating an address" elements of Claim 13.

Cirrus, relying on CX 61C, CX 62C, Mr. Schafer's testimony, (Schafer, Tr. at 590), and Mr. Ferraro's Supplemental Report at CX 745C, next alleges that the 5465 meets the "circuitry for selectively retrieving" limitation of Claim 13. In this regard, Cirrus contends that the memory controller of the 5465 selectively retrieves data from on-screen memory in order to refresh the display screen and selectively retrieves video data from the off-screen region in order to refresh the overlay window on the screen. Cirrus also contends that it has presented documentation showing that the 5465 retrieves both video and graphics data during the active raster scan thereby meeting the "as data is rastered" portion of this claim limitation.

The "selectively retrieving" element, as discussed *infra* in claim construction, requires a selection between video and graphics data in the retrieval process, which retrieval may occur anytime during the entire rastering process, including both the active raster scan and the retrace period.

ATI again raises no contentions in either its Post-Hearing Brief or Reply Brief specifically disputing Cirrus' claim that the 5465 product meets the "circuitry for selectively retrieving" limitation of Claim 13, but as referenced in the introductory portion of this section,

ATI contests the sufficiency of CX 61C and CX 62C and Mr. Ferraro's reliance on CX 61C. I reject ATI's argument for the reasons set forth above, and find that the evidence cited by Cirrus is sufficient to establish that the 5465 selectively retrieves video and graphics data during rastering, based on Mr. Schafer's testimony that indicated the 5465 can selectively retrieve graphics or video data as necessary for the display, Schafer, Tr. at 589-90, and the expert opinion on "as ... rastered" expressed by Mr. Ferraro who, as someone skilled in the art, apparently deemed his information on this Cirrus product, including CX 61C, sufficient to discern that this limitation was met.

Cirrus next states that the 5465 contains the graphics and video backend pipeline elements of Claim 13 as it contains a graphics backend pipeline used primarily for formatting data retrieved from the frame buffer[4] to create an RGB pixel stream that is output to a display, and it has a separate video backend pipeline that accepts as input pixel data from the frame buffer through the memory controller and provides as output formatted video pixels for display. As construed, *infra*, the graphics and video backend pipelines taught by the '525 Patent are separate and do not share any elements or circuitry. The first pipeline processes for display graphics data retrieved from the frame buffer while the second pipeline processes for display video data.

In asserting that the 5465 meets the video pipeline and graphics pipeline elements of Claim 13, Cirrus relies on the testimony of Mr. Schafer that the 5465 has separate backend graphics and video pipelines that perform the above-noted functions. Schafer, Tr. at 585-86.

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[4] The issue of whether the 5465 meets the frame buffer limitation of Claim 13 is discussed *supra*.

Cirrus also relies on CX 61C, CX 62C and the Supplemental Report of Mr. Ferraro, (CX 745C at 99-101).

ATI, in its response to Cirrus' Proposed Findings of Fact, challenges the sufficiency of this evidence, contending first that while Mr. Schafer initially testified that the graphics and video pipelines were separate on the 5465, he corrected his testimony stating "they were not". Based on a review of the questions asked of Mr. Schafer and his responses thereto, I find the record, Tr. at 586-87, does not support ATI's allegation that Mr. Schafer changed his testimony, and I therefore conclude that Mr. Schafer's testimony supports a finding that the 5465 meets the graphics and video backend pipeline elements of Claim 13. Additionally, I reject ATI's repeated challenge to the sufficiency of CX 61C and CX 62C as support for Mr. Ferraro's opinion for the reasons set forth above. I therefore find that Cirrus has met its burden of demonstrating that the 5465 contains the requisite graphics and video backend pipelines.

Cirrus maintains that the 5465 meets the "always rastering" graphics element of Claim 13, asserting that the 5465 operates in a mode allowing for occlusion and that in this mode, on-screen graphics pixels are always rastered out for every pixel location on the screen regardless of whether the display is in a window or not. See CX 62C at CL 89103 ("If occlusion is being used, pixels are fetched from both sources so that either the background or window can be displayed.") Cirrus further alleges that generally the 5465 rasters all of the graphics pixels out of the frame buffer for each scan line. As support for its contention that this element of Claim 13 is met, Cirrus cites the testimony of Mr. Schafer, Tr. at 591, and the 5465 Technical manual, CX 62C at CL89103, 89106.

ATI alleges that the 5465 does not satisfy the "always rastering" requirement of Claim 13 because it does not continually retrieve graphics data from the frame buffer at a steady rate and without interruption. In construing, *infra,* the "always rastering" element of Claim 13, I have concluded that it allows for some minor engineering delays and that nothing in the architecture of the '525 Patent suggests that "always rastering" is to be accomplished only by retrieval "continuously at a steady rate." In view of the evidence cited by Cirrus, I conclude that the rastering of data to the graphics pipeline is ongoing in the 5465. Furthermore, I note that ATI's argument in opposition to Cirrus' contention that this element is met is based on what I have found to be faulty claim construction. I find therefore that the 5465 meets this limitation of Claim 13.

Cirrus also argues that the 5465 meets the "when" condition of Claim 13. As noted previously, and as set forth in the claim construction section *infra,* this condition is fatally indefinite, thereby rendering Claim 13 invalid.

Cirrus last argues that the 5465 contains the output selector circuitry element of Claim 13. The parties have not disputed the meaning of this element, so I have accorded it its ordinary, plain meaning. Mr. Schafer testified that the 5465 has a multiplexer to which the graphics and video pipelines provide data, and that the multiplexer is controlled by a circuit which uses video window position information and color keying to determine for each pixel location whether video or graphics data will be passed. Schafer, Tr. at 582, 591. Inasmuch as ATI does not advance any specific contentions in its briefs that this evidence relied upon by Cirrus does not establish that the 5465 satisfies the output selector circuitry element, I find this element met.

In sum, I have found that the 5465, upon which Cirrus' domestic industry claim is based, does not practice Claim 13 as it lacks the required frame buffer and does not meet the first port limitation, and that, in any event, the "when" limitation of Claim 13 is fatally indefinite and renders invalid Claim 13, the only claim Cirrus relied on in advancing its domestic industry argument. I therefore find that Cirrus has failed to establish that it meets the technical prong of the domestic industry requirement.

II. Infringement

An infringement analysis involves two steps: first, construction of the claim asserted to be infringed to determine its meaning and scope, and second, comparison of the properly construed claim to the accused product or process. Tanabe Seiyaku Co. v. U.S. Int'l Trade Comm'n, 109 F.3d 726 (Fed. Cir.), cert. denied, 118 S.Ct. 624 (1997); Markman v. Westview Instruments, Inc., 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc), aff'd, 517 U.S. 370 (1996). The burden rests on the patent owner to establish infringement by a preponderance of the evidence. SmithKline Diagnostics Inc. v. Helena Lab. Corp., 859 F.2d 878, 889 (Fed. Cir. 1988). The patent owner must show that for each patent claim asserted, the accused process or product satisfies every claim limitation, either literally or under the doctrine of equivalents. Id. For the reasons that follow, I conclude that the ATI Rage Devices do not infringe the asserted claims of the '525 Patent.

A. Claim Construction

The meaning and scope of a patent claim should be determined with reference to the claim language, the specification, and the prosecution history. Extrinsic evidence outside the record before the Patent and Trademark Office (PTO), such as expert testimony about how

those skilled in the art would interpret certain language in the claim, may also be considered when appropriate as an inherent part of the process of claim construction and as an aid in arriving at the proper construction of the claim. Tanabe, 109 F.3d at 732; Markman, 52 F.3d at 979.

1. Claims 13 and 37

Claim 13 of the '525 Patent teaches the following:

13. A controller comprising:

circuitry for writing selectively each word of received data into [a] selected one of on-screen and off-screen memory spaces of a frame buffer;

a first port for receiving video and graphics data, a word of said data received with an address of said memory spaces directing said word to be processed as a word of video data or a word of graphics data;

a second port for receiving real-time video data;

circuitry for generating an address associated with a selected one of said memory spaces for a word of said real-time video data;

circuitry for selectively retrieving said words of data from said on-screen and off-screen memory spaces as data is rastered for driving a display;

a graphics backend pipeline for processing ones of said words of data representing graphics data retrieved from said frame buffer;

a video backend pipeline for processing other ones of said words of data representing video data retrieved from said frame buffer, said circuitry for retrieving always rastering a stream of data from said frame buffer to said graphics backend pipeline and rastering video data to said video backend pipeline when a display raster scan reaches a display position of a window; and

output selector circuitry for selecting for output between words of data output from said graphics backend pipeline and words of data output from said video backend pipeline.

Claim 37 of the '525 Patent teaches the following:

37. A display controller comprising:

circuitry for selectively retrieving data from an associated multi-format frame buffer for simultaneously storing graphics and video data;

a first pipeline for processing words of graphics data selectively retrieved from said frame buffer; and

a second pipeline for processing words of video data selectively retrieved from said

frame buffer.

a. Controller

The parties' dispute regarding the construction of Claim 13 and Claim 37 begins with the first words of these claims – "a" and "controller". Although the parties apparently agree on the function of a controller, as managing and regulating the functioning of the computer display, they disagree on what Cirrus terms the "structural definition" of this controller. Cirrus argues that these two words constitute a claim limitation that requires (1) a *single* controller, as opposed to multiple controllers, and (2) an integrated controller design. In support of this argument, Cirrus asserts that the use of the language, "a controller", instead of "one or more controllers" or "a display system" establishes the single integrated circuit design requirement, and that the specification of the patent is consistent with its interpretation. Cirrus also contends that the dotted line around the VGA controller depicted in Figure 2 of the '525 Patent lends credence to its position, as that figure shows a "tightly coupled, highly integrated design" and "[n]o modularity between its components is illustrated." Cirrus Post-Hearing Brief at 26. Cirrus discounts the unfavorable testimony on this issue by its own technical expert, Richard Ferraro, on the grounds that Mr. Ferraro is not a lawyer and that "he did not assess the prior art against the single integrated design limitation." Cirrus Post-Hearing Brief at 26. Cirrus offered no evidence that "a controller" would not generally be understood in the relevant industry to encompass a modular component design.

In sharp contrast, ATI argues that nothing about the claim language, "a" and "controller", requires or even suggests a single, integrated, non-modular design, so as to exclude a controller system consisting of modular components. First, ATI claims that because

the term is found in the preamble of Claim 13 and of Claim 37, it should not be considered a claim limitation, as "it does not lend life and meaning to the claim." ATI Reply Post-Hearing Brief at 13. ATI next refutes Cirrus' argument regarding the dotted line in Figure 2 of the patent, noting that the dotted line is a numbered feature merely showing the correspondence between Figure 2 and Figure 1 of the patent. As to Cirrus' abandonment of Mr. Ferraro's testimony on this subject, ATI maintains that Cirrus cannot pick and choose only the favorable testimony of its expert, on whom it relied exclusively for its pre-hearing claim construction, and on whom it continues to rely for more favorable testimony. Finally, ATI argues that the plain language of this portion of the claim supports its interpretation, as does a review of other Cirrus patents which specifically claim a single integrated circuit or chip in just such explicit terms.

The Staff takes the position that the "a controller" claim language should not be construed to require a single integrated circuit design, arguing that nothing in the language of Claim 13, Claim 37 or in the drawing of Figure 2 supports such an interpretation. In response to Cirrus' contention that "a" connotes an integrated design, the Staff argues that such usage of "a" in Claims 13 and 37 is merely a convention of patent drafting, and that "a" also covers more than one, citing Landis on Mechanics of Patent Claim Drafting (4th ed. 1997), § 20, p.III-18 for this proposition, and also pointing out other usages of "a" and "an" in the '525 Patent which the Staff argues obviously refer to the plural as well as to the singular. The Staff indicates that nothing in the prosecution history of the '525 Patent supports Cirrus' interpretation. In light of these factors and Mr. Ferraro's testimony that no such limitation exists in the '525 Patent, the Staff concludes that "a controller" should be construed to allow

for modular component controllers as well as those with a single integrated circuit design.

A review of the '525 Patent in its entirety indicates that the language, "a controller", in the preamble of Claim 13 and Claim 37 should be considered a limitation, rather than mere introductory language, and ATI's argument against consideration of the language must be rejected. This language certainly gives meaning and an important context to the claims, helps define the invention and appears repeatedly throughout the '525 Patent. See In re Paulsen, 30 F.3d 1475 (Fed. Cir. 1994) (deeming preamble language a claim limitation where the words give meaning to the claim); Gerber Garment Tech, Inc. v. Lectra Systems Inc., 916 F.2d 683 (Fed. Cir. 1990) ("Where words in the preamble 'are necessary to give meaning to the claim and properly define the invention,' they are deemed limitations of the claim"); Perkin Elmer Corp. v. Computervision Corp., 732 F.2d 888 (Fed. Cir.), cert. denied, 469 U.S. 857 (1984) (finding claim limitations in the preamble where "...necessary to give meaning to the claim and properly define the invention").

However, consideration of the intrinsic evidence, including the language of all claims, the specifications, and the prosecution history yields no indication or even suggestion that "a" and "controller" constitutes a requirement of a single integrated circuit design. Although Cirrus argues that "a" is a singular indefinite article, the Staff correctly notes that general principles of patent drafting provide for the use of a singular article to include both singular and plural. See Abtox, Inc. v. Exitron Corp., 122 F.3d 1019 (Fed. Cir. 1997) (finding "a" to refer to the singular in light of other references in the patent and specification, but noting that "...patent claim parlance also recognizes that an article can carry the meaning of "one or more," for example in a claim using the transitional phrase "comprising""); North Am.

Vaccine Inc. v. Am. Cyanamid Co., 7 F.3d 1571 (Fed. Cir.), cert. denied, 114 S.Ct. 1645 (1993) (noting that "...it is generally accepted in patent parlance that "a" can mean one or more", although in that case the specification indicated a singular meaning). Abtox also suggests that where, as in Claim 13 and in Claim 37, "a" is coupled with the transitional phrase, "comprising", this often indicates a plural as well as singular meaning. Considering the '525 Patent in its entirety, no support can be found elsewhere in the patent for the construction of "a controller" advocated by Cirrus. As to Cirrus' argument concerning the dotted line in Figure 2 of the '525 Patent, an examination of Figures 1 and 2 of the patent shows that the dotted line does not represent the integrated nature of the design, but rather shows the relationship between what is represented in the two figures.

Furthermore, even considering extrinsic evidence on construction of this claim element, expert testimony of record regarding the meaning of this claim term, including that of Cirrus' own technical expert, Mr. Ferraro, supports construction of the term to include modular component controllers as well as those of a single integrated circuit design. Ultimately, a court must construe the claim language according to the standard of what those words would have meant to one skilled in the art as of the application date. W. L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1556, (Fed. Cir. 1983); see also York Prods., Inc. v. Central Tractor Farm & Family Ctr., 99 F.3d 1568, 1572 (Fed. Cir. 1996) ("Without an express intent to impart a novel meaning to claim terms, an inventor's claim terms take on their ordinary meaning"). In light of this evidence, Cirrus' proposed construction of "a controller" must be rejected, as the term covers not only a unitary integrated design, but also a modular component design.

b. Frame Buffer/Multi-Format Frame Buffer

The parties next raise a dispute regarding the construction of "frame buffer" in Claim 13 and "multi-format frame buffer" in Claim 37, with Cirrus, ATI and the Staff all taking divergent positions on this issue. Cirrus and ATI agree that "frame buffer" and "multi-format frame buffer" share the same meaning, but Cirrus and ATI disagree as to what that shared meaning is. The Staff maintains that these two terms have different meanings.

Cirrus claims that in the '525 Patent both these terms refer to memory holding information for ultimate display, where such memory is divided into an on-screen and an off-screen region and holds video and graphics data in their native formats. Cirrus maintains that no requirement exists in Claim 13 or Claim 37 that the frame buffer or multi-format frame buffer simultaneously store both graphics *and* video data in the same region of the memory. Cirrus notes that the specification, Column 6, lines 17-19, states "[e]ach space [of the frame buffer] can simultaneously store graphics *or* video data depending on the selected display configuration" (emphasis added)[5]. Cirrus contends that the specification and the prosecution history support its proposed construction, and that the contrasting language of Claim 25 ("multi-format frame buffer memory having on-screen and off-screen areas each operable to simultaneously store data in graphics and video formats") and Claim 43 ("multi-format frame buffer having on-screen and off-screen areas each for simultaneously storing both graphics and video pixel data") also supports its position.

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[5]Cirrus' expert, Mr. Ferraro, when opining on the "multi-format frame buffer" that he and Cirrus contend share the same meaning as the "frame buffer", stated, "I also understand that graphics data can reside in either on-screen or off-screen memory and video data can reside in either on-screen or off-screen memory." CX 745C at 77 (Ferraro Rebuttal Report).

ATI asserts that although "frame buffer" and "multi-format frame buffer" share an identical meaning, they refer to memory divided into an on-screen and an off-screen region where each region simultaneously stores graphics and video data. ATI argues that this construction is consistent with the specification and with Cirrus' representations to the Patent Office during prosecution of the '525 Patent that its frame buffer was different from that in the Siann '306 Patent, which ATI maintains is identical to the frame buffer in its accused products. Cirrus notes that the portion of the specification cited by ATI refers to just one possible configuration mode of the frame buffer, and disputes ATI's characterization of its statements to the Patent Office.

The Staff takes the position that "frame buffer" as used in Claim 13 refers to "a block of memory, logically divided into at least two areas, for storing a raster image." Staff Post-Hearing Brief at 19. The Staff asserts that each of the areas can *either* store graphics *or* video data, with the use of "simultaneously" ... "or" in the aforementioned portion of the specification referring to one area storing graphics data at the same time that the other area stores video data.[6] In discounting ATI's proposed construction of the term "frame buffer", the Staff, like Cirrus, contends that the portion of the specification cited by ATI describes the multi-format frame buffer called for in Claims 25 and 37, and cannot be applied to Claim 13. The Staff further argues that ATI cannot rely on the comments in the prosecution history both because ATI's proposed construction is contrary to the plain language of the specification and

[6]In the claim construction section of its brief, the Staff seems to suggest that each area of the frame buffer must be able to store graphics or video, although not simultaneously in the same area. However, the Staff's application of the "frame buffer" element in the '525 Patent to the 5465 and the ATI Rage Products seems to suggest that the Staff may not advocate such an interpretation. Ultimately, its position remains unclear on this point.

because no direct statement was made to the Patent Office that the comments applied to all claims. Turning to the definition of "multi-format frame buffer" in Claims 25 and 43 of the '525 Patent, the Staff asserts that "multi-format frame buffer" should be construed as having on-screen and off-screen areas of memory that *each* simultaneously store graphics *and* video data. The Staff relies on the doctrine of claim differentiation to support its argument that the adjective "multi-format" renders the multi-format frame buffer of Claim 37 more narrow than the frame buffer of Claim 13, and that this limitation from Claim 37 should not be read into Claim 13.

Based on the plain language of the claims and the specification, a distinction exists between the terms "frame buffer" and "multi-format frame buffer". Interspersed throughout the '525 Patent, the drafter repeatedly uses both terms, with "frame buffer" in certain places, and "multi-format frame buffer" in others, suggesting some intent to distinguish between them. The generally accepted meaning of "frame buffer", a memory space, does not include the limitations proposed by ATI, and nothing in the '525 Patent indicates that it should be given a definition that incorporates such limitations. While Claim 13 makes clear that its frame buffer has two distinct storage areas (on-screen and off-screen), and that each of the areas can store either graphics or video ("[e]ach space [of the frame buffer] can simultaneously store graphics *or* video data depending on the selected display configuration", CX 1, Column 6, lines 17-19), the claim language and specification do not support imposing the limitation that each area in the "frame buffer" *simultaneously* store both graphics *and* video data. While each of the memory areas of the "frame buffer" should have the ability to store either type of data, each area need not store both forms of data at the same time. The contrasting language from Claims

25 and 43 regarding the "multi-format frame buffer" buttresses this finding, as those claims show the drafter of the '525 Patent clearly specifying simultaneous graphics and video data storage in a single region of the frame buffer when the drafter wished to convey that concept.

The "multi-format frame buffer" refers to a memory having on-screen and off-screen areas that *each* can simultaneously store both graphics and video data.[7] The definitions of "multi-format frame buffer" in Claims 25 and 43 support this construction. See Fonar Corp. v. Johnson & Johnson, 821 F.2d 627, 632 (Fed. Cir.), cert. denied, 484 U.S. 1027 (1988) (holding that the same term should be give a consistent meaning throughout the patent). Also the adjective "multi-format" should be given some meaning, instead of being read out of the claim, as both ATI's and Cirrus' identical meaning arguments require. The '525 Patent specification contemplates different, alternate configurations of the frame buffer, which again bolsters the concept of a distinction between a "frame buffer" and a "multi-format frame buffer". See CX 1, Column 6, lines 30-32 ("According to the principles of the present invention, there are alternate ways of storing and retrieving graphics and video data from

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[7]I note that Claim 40, which depends on Claim 37, adds the limitation "...wherein said frame buffer is partitioned into on-screen and off-screen areas, each of said on-screen and off-screen areas operable to simultaneously store both graphics and video data." While no party raises this issue, arguably, the doctrine of claim differentiation, as applied to Claims 37 and 40, might support a different construction of "multi-format frame buffer" than the one I am giving it. However, any other interpretation than that adopted would run counter to other claim construction principles and the '525 Patent specification, and I conclude that considering the '525 Patent in its entirety, and considering all applicable doctrines for claim construction, this construction of "multi-format frame buffer" is correct notwithstanding Claim 40. See Moleculon Research Corp. v. CBS, Inc., 793 F.2d 1261, 1269 n.4 (Fed. Cir.), cert. denied, 479 U.S. 1030 (1987) (upholding construction of independent claim that rendered dependent claim redundant, where the patent in its entirety supported the construction); Texas Co. v. Globe Oil & Refining Co., 112 F. Supp. 455, 467 (N.D. Ill.), aff'd, 225 F.2d 725 (7th Cir. 1955) (holding claim differentiation inapplicable where resulting construction would "measure an invention different and contrary to that disclosed in the specifications").

unified frame buffer 107). Cirrus' statements to the Patent Office, found in the prosecution history, that the frame buffer in the claimed invention differed from that in the Siann '306 Patent does not dictate the claim construction on these terms as Cirrus did not characterize the nature of the claimed frame buffer. Furthermore, the claim language and the specification, which take precedence over other evidence, make the meaning of the terms apparent. See Digital Biometrics, Inc. v. Identix, Inc., 149 F.3d 1335, 1344 (Fed. Cir. 1998) ("Even within the intrinsic evidence, however, there is a hierarchy of analytical tools" with the actual words of the claim and the specification at the top).

c. Circuitry for Writing Selectively...

The parties agree that the circuitry for writing taught by Claim 13 refers to circuitry for writing data into memory, but the parties disagree as to the meaning of the modifier, "selectively" in this limitation of the claim. Cirrus argues that this means that the circuitry, in writing data into memory, can select between the on-screen region and the off-screen region, as appropriate according to the address of the word of data, and that data is written on a word-by-word basis, rather than being written as a group. Cirrus asserts some support for its proposed construction in the abstract of the patent: "Circuitry 200, 201, 202, 207, 208 is provided for writing a word of the pixel data received from the interface 206 to a one of the on- and off-screen memory areas corresponding to the address associated with the received word." ATI maintains that the circuitry must write data into either on-screen or off-screen memory, selecting between them based on "some criteria", but ATI contends that this criteria is never defined by the patent. ATI also criticizes Cirrus' "word-by-word" construction as unsupported by the record.

The record supports the construction of "circuitry for writing selectively" as referring to the selection between on-screen and off-screen memory as data is written into the frame buffer. As an initial matter, I note that the plain meaning of the above-referenced language from the abstract relied on by Cirrus would not indicate that "selectively" is used to refer to writing on a word-by-word basis, although the abstract certainly describes an individual word of data being written. Instead, Claim 13 and the '525 Patent specification, including the abstract, plainly indicate that "selectively" refers to a selection between the two memory areas, according to the address. Given that the patent itself is not ambiguous on this issue, there is no need to resort to expert testimony in interpreting it, rendering unpersuasive Cirrus' citation of a conclusory statement by Mr. Ferraro, interpreting the claim limitation to mean that "word-by-word" writing is performed.

As to ATI's proposed construction, I find that it unnecessarily leaves the claim vulnerable to indefiniteness and enablement problems, while the adopted construction, which finds support in the specification, including the abstract of the patent, does not.[8] It is appropriate to ascertain the meaning of a claim in light of the patent as a whole, and a review of the '525 Patent in its entirety supports interpreting "selectively" as referring to a selection between off-screen and on-screen memory based on the address of the word of data. See Loctite Corp. v. Ultraseal Ltd., 781 F.2d 861, 867 (Fed. Cir. 1986) (finding true meaning of

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[8]ATI asserts that the abstract should not be considered in claim interpretation, relying on 37 C.F.R. § 1.72(b), but notwithstanding, the abstract is part of the specification and is considered part of the patent disclosure. Application of Armbruster, 512 F.2d 676, 678 (C.C.P.A. 1975); See also Kaspar Wire Works, Inc. v. K-Jack Eng. Co., Inc., 1995 WL 662674 at **2 (Fed. Cir. 1995) (unpublished disposition) (relying on the patent abstract to interpret claim term).

claim by interpreting based on the specification and the patent as a whole).

d. A First Port ...

The parties also take opposing views on the "first port" limitation of Claim 13. All the parties agree that the port is an external interface, but their positions diverge regarding the precise characteristics of the "first port" taught by Claim 13. Cirrus, relying in part on Mr. Ferraro's testimony, claims that the first port receives words of data, each with an accompanying address that, by directing to the appropriate memory space, directs whether the word should be processed as video or graphics data. Cirrus maintains that the port can write the data directly to the frame buffer based on the received address, without the port itself performing any "frontend" processing or having any independent recognition of the video or graphics nature of each word of data. ATI, on the other hand, argues that the port uses the address to perform some "decoding" or frontend processing on the words of data to determine whether the data received is graphics or video. The Staff's position on this "first port" dispute remains unclear, with the Staff merely stating that the first port "...utilizes the address associated with the data entering through the first port to direct the data for processing as either graphics data or video data." Staff Post-Hearing Brief at 21. ATI relies heavily on the specification of the patent in support of its position, citing Column 5, lines 52 - 62. Cirrus relies primarily on the claim language to support its view, and cites the doctrine of claim differentiation to refute what it contends is ATI's argument that the first port must be a dual aperture port; Claim 24 of the '525 Patent teaches "[t]he controller of claim 13 wherein said first por[t] comprises a dual-aperture port." ATI replies that the dual aperture port is consistent with its proposed claim construction, but not required.

I find that, as claimed by ATI, the "first port" described in Claim 13 receives data with accompanying addresses that indicate its character as either graphics or video and decodes the addresses to direct the data for processing as video or graphics data before the data is placed in the frame buffer. This construction is consistent with the claim language, and with the description of the preferred embodiment set forth in the specification at Column 5, lines 51-65. The testimony of Mr. Schafer, one of the '525 Patent inventors, on this point further supports this construction, as he testified that the first port limitation concerned the host interface receiving words of data, and before the data is written to the frame buffer, decoding the addresses on the words of data, and passing them according to the address for appropriate frontend processing. Schafer, Tr. at 660-64. Additionally, while Cirrus relies as support for its challenge to ATI's proposed claim construction on Mr. Ferraro's testimony that the spaces in memory direct the word to be processed as video or graphics, this reliance is misplaced because as construed, *supra,* the memory areas of the frame buffer of Claim 13 of the '525 Patent have the ability to store either graphics or video data and therefore the position in memory alone will not direct the words to the appropriate pipeline. Further, I note that, as ATI points out, Cirrus in its Prehearing Brief admitted that Claim 13 "requires a first port through which data is received with addresses that tell the claimed device whether the data is video or graphics so that it will be properly processed." Cirrus Prehearing Brief at 25. [9]

e. Second Port... and Circuitry for Generating an Address...

The constructions of the "second port..." and "circuitry for generating an address..."

[9] As to Cirrus' argument that ATI's proposed claim construction improperly requires a dual aperture port, ATI, as noted previously, argues consistent with Mr. Schafer's testimony on this precise point, Schafer, Tr. at 664, that a dual aperture port is not required.

limitations of Claim 13 are not points of contention among the parties. This external interface receives video data from a "real-time" source. Because the "real-time" video data lacks addresses, addresses must be generated for this data in order to write it into the frame buffer. Claim 13 teaches circuitry to generate such addresses.

f. Circuitry for Selectively Retrieving...

Both Claims 13 and 37 contain limitations as to circuitry for the selective retrieval of data. Cirrus maintains that the circuitry for selectively retrieving refers to circuitry having the ability to fetch video and graphics data on a "word-by-word" or "chunk-by-chunk" basis, rather than on an entire frame basis. Cirrus asserts, for example, that "word 100" could be retrieved following "word 1", instead of being forced to retrieve "word 2" after "word 1". Cirrus Proposed Finding of Fact 377. In support of this interpretation, which is not obvious from the plain language of the claim or from the specification, Cirrus relies on a conclusory statement by Mr. Ferraro, who provides no explanation or support for his opinion on the meaning of "selectively". Claim 13 teaches the further limitation that the selective retrieval occurs "as data is rastered for driving a display". Cirrus claims that this means that "...the circuitry for retrieving must retrieve data from both the off-screen and the on-screen regions during the active raster scan". Cirrus Post-Hearing Brief at 38. Cirrus also notes that, in this context, "rastered" should be defined as "...providing data for purposes of illuminating the pixel locations in a sequential fashion, left to right, top to bottom." Cirrus Post-Hearing Brief at 38.[10]

[10]ATI and the Staff point out that "rastered" is not typically used in relation to a memory operation. They acknowledge, however, that the traditional meaning of "rastered" clearly does not fit its use here.

With regard to both these claim limitations, ATI initially offers argument that they cannot be construed, but instead must fail for indefiniteness. Specifically, ATI asserts that the absence of an articulated selection criteria for the retrieval renders the claim elements invalid. Also, as to Claim 13's limitation, ATI maintains that "said words of data" lacks a clear antecedent, rendering it indefinite on that basis.[11] I do not find these indefiniteness arguments persuasive, and instead conclude that these claim limitations meet the definiteness requirement, and can be construed and applied, as set forth below.

ATI additionally disagrees with Cirrus' limitation on "as ... rastered" as allowing for retrieval only during the active raster scan or refresh period of the display, and not during the retrace periods. ATI Reply Brief at 24. ATI relies for support on testimony by one of the inventors of the '525 Patent, Robert Nally, but Cirrus responds that Mr. Nally's testimony cannot be applied to this issue, as he was discussing the meaning of "rastering" out of context. ATI claims that Cirrus offers a contorted construction of this limitation in an attempt to avoid the prior art, and that Cirrus' attempt to read the "as" language as requiring memory retrieval only during the active scan of the period "with no delays, no overlap, no 'engineering realities'" is inconsistent with its proposed construction of the "when" limitation. The Staff does not directly address this dispute between the parties, but notes that this limitation should be construed to call for "the retrieval of individual words of data as data is being retrieved for purposes of refreshing the display."

In Claims 13 and 37, the selective retrieval of data refers to the selection between

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[11]ATI further states, however, that although in its view this element remains indefinite and unclear, it does not dispute Cirrus' proposed assertion that the "data" referenced includes both graphics data and video data.

graphics and video data stored in the two areas of the frame buffer. Cirrus' proposed construction of "selectively" as referring to the retrieval of words of data "out of order" finds no support within the '525 Patent, and seems to be supported only by the assertion of Mr. Ferraro, who provides no rationale for this understanding. He did not offer, for example, testimony that "selectively" holds this special meaning in the art. Based on the plain language of these claims, in the context of the '525 Patent as a whole, "selectively" indicates that the retrieval of data involves choosing between graphics and video data, such that the claims cover circuitry having the ability to retrieve selectively between graphics and video, regardless of the precise nature or functionality of that circuitry. In this regard, I note that the '525 Patent teaches separate video and graphics pipelines for processing data, indicating that data from the on-screen and off-screen areas of the frame buffer is generally segregated by type for backend processing. Because the frame buffer is undifferentiated, and can store either type of data in either of its memory areas, the selection inherent in "selectively" retrieving includes selecting between video and graphics data. Mr. Schafer supported this interpretation of "selectively" as referring to the selection between graphics and video. Schafer, Tr. at 666-67. The '525 Patent elsewhere discloses mechanisms for making this choice, and evidence in the record indicates that such mechanisms were well-known in the art.

This limitation of Claim 13 also requires the selective retrieval of graphics and video data to occur as data is being provided to illuminate the screen display, which process, in its totality, includes both the active raster scan and the horizontal retrace periods. The record supports a finding that one skilled in the art would understand the reference to "as ... rastered" this way, and would not understand it to exclude the retrace periods and include only the active

raster scan. Instead, as indicated by Mr. Nally, one of the inventors, the term "raster" typically connotes the entire process, not just the active raster scan. Nally, Tr. at 174-75. From the standpoint of one skilled in the art, engineering realities such as the horizontal retrace periods are inherent in the process. Thus, where nothing in this limitation of Claim 13 explicitly limits "as ... rastered" to only the time during the active raster scan, the imposition of such a narrow reading would be inappropriate.

g. A Graphics Backend Pipeline.../A First Pipeline...

All parties agree that a "pipeline", a term common to both Claim 13 and Claim 37, refers to a sequence of processing stages where the output of one becomes the input of another, and so on, in "assembly line" fashion. They also concur on the meaning of "backend" as referring to circuitry between the frame buffer and the output circuitry. However, while Cirrus contends that even though Claim 37 does not include the word "backend", the "first pipeline" of Claim 37 is a backend pipeline, ATI disagrees that such an element exists in the "first pipeline" limitation of Claim 37, and the Staff takes no position on this issue.

A review of the plain language of Claim 37 indicates that the "first pipeline" described therein is a backend pipeline, according to the definition of that term agreed on by the parties. The "first pipeline" processes for display graphics data retrieved from the frame buffer. Therefore, it constitutes circuitry between the frame buffer and the output circuitry, meeting the parties' definition of "backend".

h. A Video Backend Pipeline.../A Second Pipeline

From these limitations of Claim 13 and Claim 37, Cirrus raises the point that, based on the prosecution history and the specification of the '525 Patent, the graphics pipeline and the

video pipeline constitute *distinct* pipelines that cannot share elements or circuitry. Apart from the claim language, Cirrus relies on a statement in its first Information Disclosure Statement ("IDS") distinguishing prior art as not disclosing "a pair of output pipelines for separately processing graphics (RGB) and video (YUV) data retrieved from the single frame buffer." ATI deems Cirrus' contention erroneous, and argues that the specification supports allowing the graphics and the video pipelines to share elements, citing examples of "shared use" in the '525 Patent. ATI claims that the specification demonstrates that the two pipelines in the '525 Patent share a FIFO (first-in, first-out storage), such that shared circuitry is clearly contemplated by the patent.[12] Cirrus denies that this FIFO is "shared", as ATI refers to descriptions of "two entirely different implementations", one in which the FIFO is the frontend processing circuitry, and the other in which the FIFO is in the backend video pipeline; Cirrus asserts that this FIFO is never part of the backend graphics pipeline. A review of the figures in the '525 Patent supports Cirrus' assertion that the pipelines shown do not share a FIFO, or any other elements.

Because Claim 13 and Claim 37 set forth separate limitations for the graphics pipeline and the video pipeline, because no part of the patent references or suggests any shared elements, and because in the prosecution history, the first IDS describes the *separate* processing of graphics and video data, I conclude that this limitation does not allow for the

[12]While ATI challenges here Cirrus' proposed claim construction, I note that ATI subsequently appears to concede that the graphics and video pipelines must constitute *distinct* pipelines. See ATI Reply Brief at 48 wherein ATI argues that Cirrus failed to prove that it was entitled to an invention date prior to the filing of the '525 Patent application because Cirrus failed to establish that it conceived and reduced to practice certain features of the patent claims, including, ATI argues, "separate and distinct pipeline circuitry (claims 13 and 37)".

pipelines to share elements. ATI offers no reliable support in the record for construing the graphics and video pipeline elements as sharing circuitry, and at the hearing, no party offered explicit testimony regarding the understanding of one skilled in the art as to whether two such distinctly identified pipelines with different functions might share some of the same circuitry. Based on the separate identification and functioning of the pipelines, the prosecution history of the '525 Patent, and on the absence of any contrary suggestion elsewhere in the patent, Claim 13 and Claim 37 are construed to teach separate and distinct dual pipelines that do not share any elements.

i. Always Rastering ...

The parties next raise a dispute as to the meaning of Claim 13's limitation that the circuitry for retrieving is "always rastering a stream of data" from the frame buffer to the graphics pipeline. Cirrus claims that the atypical usage of rastering applies here, referring to the retrieval of data from memory for the purposes of ultimately providing it to the display. In this context, Cirrus asserts that "always rastering" means "...retriev[ing] a graphics pixel for every illuminated pixel location on the screen regardless of whether the graphics data might be occluded by other display data." Cirrus Post-Hearing Brief at 40. Cirrus argues that the specification supports this construction of an ongoing stream of graphics data to the graphics pipeline. ATI proposes a construction of "always rastering" as requiring the circuitry for retrieving to "continuously provide data to the graphics stream without interruption and at a steady rate". ATI Prehearing Brief at 66. Although ATI concludes in its Reply Brief that Cirrus agrees with its definition, Cirrus claims that ATI's argument that the "always rastering" must occur at a continuously steady rate cannot be accepted. Cirrus maintains that the

specification, Column 9, lines 57-67, describes interruptions in the retrieval to the graphics pipeline "by requests from the video pipeline that steal graphics retrieval cycles", such that the patent specification directly contradicts a "continuously steady rate" interpretation. Cirrus Reply Brief at 19. The Staff takes no position on this issue.

The record supports the construction of "always rastering" proposed by Cirrus. A review of the specification discloses that there are certain minimal delays or interruptions in the retrieval of data and I conclude that the phase "always rastering", of necessity, contemplates the occurrence of these minimal delays.

The specification provides that the controller "... maintains a constant stream of graphics data into graphics backend pipeline 205 from memory". CX 1, Column 8, lines 24-25. It adds that "data is continuously pipelined from on-screen memory through graphics back-end pipeline 205 to the inputs of multiplexer 231". CX 1, Column 9, lines 43-46. As Cirrus notes, however, the specification further provides:

> In order to insure that graphics memory data continues to be provided to graphics backend pipeline 205, video window display controls 222 "steal' page cycles between page accesses to the graphics memory. It should be noted that once the window has been reached the frequency of cycles used to retrieve window data increases over the number used to fill the video FIFOs when outside a window. When the frequency of window page accesses increases, video window display controls 222/arbiter 221 preferably 'steal' cycles from page cycle being used to write data into the frame buffer.

CX 1, Column 9, lines 57-67.

As argued by Cirrus, these changes in the frequency of cycles used to retrieve window data and the attendant cycle stealing operate to cause delays in the retrieval of data from the

graphics pipeline. Also noted by Cirrus is that the specification provides that the memory retrieval circuitry has an arbiter which receives competing requests for memory access, including requests from the graphics pipeline. CX 1, Column 8, lines 7-14. In explaining this aspect of the controller, Mr. Bicevskis, witness for ATI, confirmed that this was the function of the arbiter and further testified that some of the requesters have to wait while the arbiter decides to give priority to another requester. He added that this would result in delays in the retrieval of data and that this would be true for any controller that uses DRAM. Tr. at 299-301. While referencing the general language of the specification pertaining to a constant stream of data and data being continuously pipelined, and arguing for a plain meaning construction of the phase "always rastering", ATI does not address the frequency of cycles used to retrieve window data, cycle stealing, or the role of the arbiter, each of which has a significant impact on the retrieval of data, as previously discussed.

Cirrus, on the other hand, has articulated a sound basis for concluding that "always rastering" allows for some minor delays or interruptions. Under these circumstances, and considering the relevant specification language as well as the testimony at the hearing, I conclude that nothing in the architecture of the '525 Patent suggests that "always rastering" is to be accomplished only by retrieval "continuously at a steady rate" as argued by ATI. ATI misconstrues the Cirrus quote it cites, distinguishing the prior art which could not retrieve both graphics and video data in parallel during the rastering process. In that passage, Cirrus is not asserting that no pauses in retrieval are allowed, or that the dual retrieval of graphics and video must occur at each and every instant, but instead is asserting that its invention can retrieve both graphics and video during the rastering process, while the prior art could only retrieve one or

the other during that time.

j. When

One of the most vigorously contested claim terms is the "when" limitation of Claim 13, which describes "...said circuitry for retrieving ... rastering video data to said video backend pipeline *when* a display raster scan reaches a display position of a window." Cirrus argues that "when" means "as needed because" or "in response to the fact that", but does not have a temporal sense of "always" or "at the exact instant." Cirrus further asserts that the meaning of "when" in Claim 13 must include certain necessary engineering delays such as for pre-fetching video data, and that interpreting "when" temporally renders a description of an engineering impossibility in the context of the patent.

ATI disagrees, and contends that "when" should be construed with a strict temporal meaning of "at the time that" or "just at the moment that". ATI relies on the specification as well as testimony by Mr. Nally and Mr. Schafer in support of its position, and cites several varying positions on the definition of "when" taken by Cirrus as an indication that Cirrus' position should be rejected. ATI claims that Cirrus' definition of "when" evolved throughout the proceeding, and was modified in order to dodge or overcome evidence unfavorable to Cirrus' infringement claim or validity position as that evidence unfolded. In fact, ATI maintains that Cirrus' current proposed construction of "when" calls for nonsensical interpretations such as "retrieving video data at a fixed delay prior to when" or "retrieving video data an unspecified number of clock cycles ahead of when".

The Staff, concurring with ATI, maintains that "when" has the temporal sense in this limitation of Claim 13 of "in the event that" or "at the time". Staff Post-Hearing Brief at 25.

Citing the specification for a comparison of the "always rastering" and the "when" limitations, Column 8, lines 17-29, and Column 9, lines 43-54, the Staff suggests that the limitation should be construed such that retrieval of video data occurs "only upon the condition that the raster scan is inside the video window." Staff Post-Hearing Brief at 26. The Staff also cites Mr. Schafer's testimony on the meaning of this limitation as supporting its interpretation. Although the Staff acknowledges Mr. Schafer's testimony that retrieval of data only during the precise time the raster scan is inside the video window did not constitute a realistic design constraint or engineering possibility, the Staff contends that an inventor's view of "design constraints" cannot alter the plain meaning of claim language and the patent specification. Additionally, the Staff argues that adopting Cirrus' proposed definition of the "when" limitation should render Claim 13 invalid under 35 U.S.C. § 112. The Staff claims that Cirrus attempts to manipulate "when" to mean "before".

Cirrus responds to ATI's criticism of its allegedly fluctuating positions by asserting that its varying formulations focused on the same "fundamental interpretation". Cirrus claims that ATI's proposed interpretation mandates a conclusion that pre-fetching is not part of rastering video data to the video pipeline. Arguing that the limitation "be read in view of its architectural purpose", Cirrus maintains that pre-fetching is part of rastering. Cirrus argues that "when" includes pre-fetching of data as part of the rastering process, and that if given a temporal sense, "when" must be loosely construed as "at the approximate time that", taking into account "predictable and unpredictable delays in retrieving and processing data." Cirrus

Post-Hearing Brief at 43.[13]

In the context of the '525 Patent in its entirety, and considering the claim terms from the standpoint of one ordinarily skilled in the art at the time of this patent, the "when" limitation of Claim 13 cannot be construed in the strictly temporal sense advocated by ATI and the Staff. Testimony by Mr. Schafer and Mr. Bicevskis, as well as expert testimony of record, indicated that at the time of the '525 Patent, one skilled in the art would certainly have known that the instantaneous retrieval of video data upon the active raster scan reaching the video window constituted an engineering impossibility. Although ATI and the Staff argue that the commonly accepted and known practical impossibility of their proposed construction should not preclude it from being adopted, I do not find these arguments persuasive. Where the patent itself discloses the occurrence of pre-fetching ("Preferably, video FIFOs 223 and 224 are filled before the raster scan actually reaches the display window ...), and where one skilled in the art would understand that this and other engineering delays are inherent in video data retrieval for display, a construction of "when" in direct contradiction thereof must be rejected.

The proper construction of "when" in light of the understanding of one skilled in the art and in light of the '525 Patent in its entirety is the commonly understood usage of "when" in a

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[13]ATI asserts in its Post-Hearing Brief that pre-fetching actually allows for the engineering feasibility of the plain meaning of the "when" limitation by permitting the video FIFOs to be filled before the raster scan reaches the display window so that the data is available immediately at the time that the raster scan reaches the window. Obviously, because ATI argues that the "when" (under its "at the exact instant" interpretation) can be met in this scenario, pre-fetching would not be considered part of rastering in this scenario. However, ATI subsequently makes an inconsistent argument in another section of its reply brief, there taking the position that pre-fetching is part of the rastering process. ATI Reply Brief at 9. Given ATI's inconsistency, and the statements in the '525 Patent specification referring to rastering *from the frame buffer*, rastering data from memory should be construed to include pre-fetching.

loose cause-and-effect sense. This portion of Claim 13 seeks to convey that the retrieval of graphics data will generally be continuous, but the retrieval of video data will occur only in connection with the display of a video window. Accordingly, the "when" limitation links the retrieval of video data with the display of a video window, such that video retrieval roughly occurs "when" a window is reached, but not necessarily at the precise instant that the window is reached. There is no other way to read the "when" limitation consistently with the specification of the '525 Patent.

However, while the experts and persons skilled in the art testified to the general understanding that pre-fetching and some engineering delays would necessarily occur, Cirrus failed to offer testimony or evidence as to the generally understood length of these delays, or the amount of time in advance that pre-fetching could occur.[14] This claim limitation would not present application or indefiniteness problems were there evidence to show some common understanding among those skilled in the art of the length of the pre-fetching and the acceptable delays. In fact, however, Cirrus' expert testified that the amount of delay or pre-fetching allowed for by Claim 13 could not be quantified. When asked to give the amount of time between the beginning of the retrieval of video data and the raster scan reaching the video window, Mr. Ferraro insisted that one skilled in the art could not make that determination from the '525 Patent itself, but rather that the determination must be "implementation-specific", changing depending on the device being compared to the '525 Patent. Ferraro, Tr. at

[14]While Dr. Peuto suggested in his testimony that an engineer considering this type of data retrieval might expect minor engineering delays of only one or two nanoseconds, this is inconsistent with Mr. Ferraro's position that an engineer would deem the more significant delays that occur in the ATI Rage Devices still fall within the "when" limitation. Peuto, Tr. at 1352; Ferraro, Tr. at 1594-96.

725. Cirrus adopts this position in arguing that "when" must "tak[e] into account predictable *and unpredictable* delays in retrieving and processing data." Cirrus Post-Hearing Brief at 43 (emphasis added). Cirrus' insistence that no boundaries can be placed on pre-fetching or retrieval and processing delays renders it impossible for one skilled in the art to interpret and apply Claim 13.[15] Accordingly, in light of the absence of testimony or evidence as to the understanding of one skilled in art regarding the "metes and bounds" of the pre-fetching and delays permitted by Claim 13, I deem the claim, and therefore its dependent claims, invalid for indefiniteness.

k. Output Selector Circuitry ...

The parties raise no dispute about the meaning of this limitation, which can be given its ordinary, plain meaning.

2. Claim 15

Claim 15 of the '525 Patent teaches the following:

15. The controller of claim 13 wherein said output selector is operable to:

in a first mode, pass only a word of data output from said graphics pipeline;
in a second mode, pass a word of data output from said video pipeline when said display raster scan has reached a display position corresponding to a window and a word of data from said graphics pipeline when said display raster scan is in any other display position;
in a third mode, pass a word of data output from said video pipeline when said display raster scan has reached a display position corresponding to a window and a corresponding word of data from said graphics pipeline matches a color key and a word of data from said graphics pipeline when said display raster scan is in any other display position; and

[15]Mr. Ferraro's testimony regarding application of the "when" limitation to the Oak/Brooktree prior art reflects the problematic uncertainty of the permissible length of delay. See Ferraro, Tr. at 779 (noting he believed it did not anticipate as to this claim limitation, but if "good arguments" were made that its delays were normal engineering delays, he might change his mind, and concluding "I'm just uncertain at this point on 13G [the "when" limitation] and the Oak/Brooktree").

in a fourth mode, pass a word of data from said video pipeline when said corresponding word of data from said graphics pipeline matches a color key and a word of data from said graphics pipeline when said display raster scan is in any other display position.

Claim 15 depends on Claim 13, and therefore faces the same indefiniteness problem, resulting from its incorporation of the "when" limitation. As to the remainder of Claim 15, there is no dispute among the parties that in the first mode, the output selector only passes graphics data. There is significant disagreement, however, between Cirrus and ATI as to what occurs in the second mode. ATI argues that this mode requires the output selector to have window position control circuitry as described in the '525 Patent specification, comparing the position of a window with the position of the raster scan. Cirrus responds that Claim 15 contains no language regarding particular types of control circuitry and that ATI's attempt to limit the circuitry to a specific circuit described in the specification violates the rule of claim construction prohibiting the reading of implementation details into the claim. Cirrus and ATI also disagree as to the construction of the "when" condition in the second mode, with Cirrus arguing that the "when" in Claim 15 connotes less temporal flexibility than the "when condition" in Claim 13, while ATI, in response to Cirrus' Proposed Findings of Fact, argues that this construction of "when" cannot be accepted because Cirrus does not quantify how much less the delay is or indicate how infringement would be avoided. The Staff advances no specific arguments as to the proper construction of the second mode of Claim 15.

With regard to the dispute over whether particular circuitry is required, I note that the specification does have language describing the circuitry of the output selector, as cited by ATI. CX 1, Column 10, lines 1-14, Column 11, line 61 through Column 12, line 35. The claim itself, however, contains no such language. While claims are to be interpreted in light of

the specifications, limitations may not be read into the claims, as noted by Cirrus. Sjolund v. Musland, 847 F.2d 1573, 1581, 6 U.S.P.Q. 2020, 2027 (Fed. Cir. 1988); Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 1571, 7 U.S.P.Q.2d 1057, 1064 (Fed. Cir.), cert. denied, 488 U.S. 218 (1988). In arguing that a particular type of circuitry is required by the second mode, ATI seeks to impose an additional limitation on Claim 15 based on language appearing in the specification. Inasmuch as this constitutes an improper importation of the specification into Claim 15, I accept Cirrus' view that there is no requirement that the output selector have the particular control circuitry advanced by ATI.

As to the meaning of "when" in the second mode, Cirrus distinguishes the term from the same term used in Claim 13 by stating that the "when" condition in Claim 15 causes an event at the output stage of the controller, whereas the "when" condition in Claim 13 refers to the retrieval of data from the frame buffer. I note, as an initial matter, that with respect to Claim 13, I found that "when" connoted rough or approximate, but not necessarily exact, temporal correspondence.

Cirrus, as support for its position, refers to testimony by Mr. Ferraro that speaking temporally, the "when" condition in the second mode of Claim 15 has less delay than the "when" condition in the case of retrieving data from the memory in Claim 13. Ferraro, Tr. at 557-558. While Mr. Ferraro stated that the passing of data would not occur instantaneously, he testified that not only was the delay here relatively shorter, but also that it was of a more predictable nature. Ferraro, Tr. at 558. ATI correctly points out that the language in Claim 13, "when a display raster scan reaches a display position of a window", is virtually identical to the language in Claim 15, "when said display raster scan has reached a display position

corresponding to a window". Notably, though, the "when" condition refers to different events in Claims 13 and 15, and whereas the specification of the '525 Patent outlines pre-fetching in connection with the "when" condition of Claim 13, the specification does not cite any such provision or delay in connection with the "when" condition of Claim 15. Furthermore, whereas with respect to Claim 13's "when" condition, Cirrus failed to establish that one skilled in the art could place "metes and bounds" on "when", here, Cirrus offers uncontested expert testimony that the amount of delay is essentially minimal and predictable from the standpoint of one skilled in the art. Practically, therefore, the boundaries of "when" in this claim can be roughly quantified based on the general understanding of one skilled in the art, and involve tighter or more strict temporal correspondence.

Consistent with my construction of Claim 13's "when" condition as calling for rough temporal correspondence and a loose cause-and-effect relationship between the two events, the '525 Patent reflects that the "when" limitation of the second mode of Claim 15 has a similar meaning, and teaches passing a word of data from the video pipeline approximately "at the time that" the display raster scan reaches a display position corresponding to a window. Because the approximation is predictable from the standpoint of one skilled in the art, this "when" limitation does not face the same indefiniteness problems as the one in Claim 13.

With respect to the third mode, the Staff offers no claim construction, while both ATI and Cirrus agree in general that this mode requires both the window position condition of the second mode and the existence of color keying. ATI takes issue with Cirrus' assertion, however, that the graphics data that is compared with the values in the color key components is not a single bit, but rather an 8, 16 or 24 bit word. As support for its position, Cirrus relies

on the language of the specification that states:

> [T]he inputs to output multiplexer 231 are ... 16 or 24-bit color data directly from graphics backend pipeline 205 serializer 236 and 24-bit color data from the color look-up table 234 ... Depending on the mode, color comparison circuitry 302 compares related bits from the overlay color key register 303 with either the 8 bits indexing look-up table 234 in the color look-up table mode (pseudo-color mode), or the 16-bits (24-bits in the alternate embodiment) passed directly from serializer 236.

'525 Patent, Column 10, lines 4-27.

ATI in response contends that Cirrus "places great emphasis that the color key operates by comparing a 'word' of graphics data to a predetermined value" in order to avoid certain alleged prior art that ATI claims performs a comparison to the most significant bit of a word of data as opposed to an entire word of graphics data. ATI further asserts that there is nothing restricting the color key to any particular combination of bits. ATI, however, advances no argument specifically challenging Cirrus' reliance on the quoted portion of the Patent specification. Considering this, as well as the fact that the plain language of the claim element at issue references a "word" of graphics data, I adopt Cirrus' proposed construction that a word of data from the graphics pipeline is compared against the color key value.

Turning to the fourth mode, the Staff provides no claim interpretation, while ATI contends that this mode should be found invalid as it attempts to mix the second half of the window position condition of the second mode with the color keying of the third mode, producing an unintelligible result. The problem, according to ATI, is that the phrase "in any other display position" is not defined, is unintelligible in relation to the "color key" recited, and has no antecedent reference. See Peuto, Tr. at 1357; Schafer, Tr. at 623-624.

Cirrus, relying on certain later testimony of Mr. Schafer, takes issue with ATI's contention as to the nonsensical nature of the description of this mode. While Cirrus first suggests that the fourth mode requires that color keying only control the passage of data ("The ATI Rage Devices Operate In a Mode In Which The Output Selector Passes Video Data In Response to Color Keying Only." Cirrus Post-Hearing Brief at 57), Cirrus subsequently offers a somewhat contradictory proposed construction, asserting that in the full-screen video mode of the ATI Rage Devices, so long as color keying is active, the claim limitation does not preclude window position control functionality (Cirrus Reply Brief at 30). Cirrus fails to explain, under this proposed construction, how the fourth mode described in Claim 15 would differ from the third mode, which details an interaction between color keying and window position control functionality.

I agree with ATI that the reference in the fourth mode to the passing of graphics data "when said display raster scan is in any other display position" is unintelligible, and renders the claim fatally indefinite. As in the third mode limitation, the use of "any *other* display position" suggests that something different occurs when the display raster scan is in a particular display position already described. In the third mode limitation, this presents no problem because that limitation includes an earlier explanation of data passing from the video pipeline "when said display raster scan has reached a display position corresponding to a window ...", such that the "any *other* display position" clearly refers to display positions other than those corresponding to a window. The fourth mode limitation, however, lacks such an antecedent reference. Cirrus attempts to escape the confusion by asserting simply that, in the fourth mode, video data is passed when the graphics data matches a color key, and graphics

data is passed whenever the color key is not matched. Cirrus Post-Hearing Brief at 57. If so, though, then the reference to the position of the display raster scan controlling the passage of graphics data in this claim limitation is completely inconsistent and/or nonsensical. The specification offers no clarification on this issue.

The inherent unintelligibility of this claim limitation was confirmed by expert testimony from the standpoint of one skilled in the art. Citing this same problematic phrase, Dr. Peuto testified that as to the description of the fourth mode, "I cannot parse it. I cannot understand it." Peuto, Tr. at 1357. Even Mr. Schafer, one of the inventors of the '525 Patent invention, stated, "It says 'in any other display position' without stating the display position. So it's confusing." Schafer, Tr. at 624.

Accordingly, I find that in addition to the indefiniteness problems stemming from Claim 15's dependence on Claim 13, Claim 15 also suffers from its own independent indefiniteness problem, and must be further deemed invalid on that basis. The nonsensical nature of the description of the fourth mode renders it impossible for one skilled in the art to understand or apply Claim 15.

3. Claim 16

Claim 16 of the '525 Patent teaches the following:

16. The controller of Claim 13 wherein said video pipeline includes a first first-in-first-out memory for receiving a plurality of words of data for a first display line of pixels in memory and a second first-in-first-out memory or receiving a plurality of words of data from a second display line of pixels in memory.

Claim 16 depends on Claim 13, again incorporating the problematic "when" limitation from that claim, and adds additional limitations in the form of a first and a second first-in-first-

out memory (FIFO). The parties agree on the commonly understood definition in the industry of "first-in-first-out memory" as a memory space where data is read out in the same order it was written in, although the patent itself provides no definition of this term. Expert testimony in the record confirms this definition. Cirrus suggests that only one other phrase in this claim, "display line of pixels in memory", requires interpretation, and contends that it should be construed to mean "the pixel data [the source data in the frame buffer] that represents the information that is going to be put on the monitor". Cirrus Post-Hearing Brief at 47. ATI argues that the phrase "display line of pixels in memory" is both nonsensical and ambiguous. If pressed for a plausible construction of the phrase, ATI proposes a definition of "that data that will make up a full horizontal row on the face of the display." ATI Post-Hearing Brief at 50. This definition is consistent with Cirrus'.

ATI raises another construction issue, however, noting the distinction between the phrases "*for* a first display line of pixels in memory" and "*from* a second display line of pixels in memory" (emphasis added). ATI, referencing figure 3 of the '525 Patent, contends this is not an error, but instead, indicates that one FIFO holds data "destined for the memory" while the second FIFO holds data "received from the memory". Cirrus denies this, arguing that the specification requires the second FIFO to operate in the backend, such that both FIFOs must be downstream from the display memory. The Staff takes no position on this dispute.

I conclude that neither of the FIFOs of Claim 16 operates as a write buffer, as suggested by ATI. Although the "for/from" distinction in the claim language raises some ambiguity as to the operation of the FIFOs, the specification makes clear that both these FIFOs operate to receive data for the generation of the on-screen display, as argued by Cirrus. See

CX 1, Column 8, lines 33-36; 44-51. I also conclude that the phrase "display line of pixels in memory" is not nonsensical, but rather is easily understood in the context of the '525 Patent, and the definition proposed by both ATI and Cirrus is correct.

4. Claim 17

Claim 17 of the '525 Patent teaches "**17.** The controller of Claim 16 wherein said first display line is stored adjacent in memory to said second display line." Dependent on Claim 16, and therefore again incorporating Claim 13's indefinite "when" limitation, Claim 17 adds to Claim 16 the limitation regarding adjacent storage. Cirrus, citing Mr. Ferraro's testimony, Ferraro, Tr. at 689, maintains that in a two-dimensional memory space, this requires storage of one display line directly above the other, and in a one-dimensional memory space, this requires the lines to be "horizontally neighboring". ATI and the Staff raise no dispute in their Post-Hearing Briefs as to this proposed interpretation, which as noted earlier, finds support in the record. Ferraro, Tr. at 689.[16] I accept the definition offered by Cirrus.

5. Claim 23

Claim 23 of the '525 Patent teaches the following:

23. The circuitry of Claim 13 wherein said video pipeline comprises:
a first-in/first-out memory for receiving a first stream of words of data from said frame buffer;
a second first-in/first-out memory disposed in parallel with said first first-in/first-out memory for receiving a second stream of words of data from said frame buffer; and
interpolation circuitry for selectively generating an additional word of data by interpolating a word of said first stream and a word of second stream data output from said first and second first-in/first-out memories.

[16]ATI merely in response to Cirrus' Proposed Findings of Fact alleges that Mr. Ferraro's statement that the lines are horizontally neighboring is unsupported. ATI points to no expert testimony of its own, however, conflicting with or challenging the opinion of Mr. Ferraro.

Claim 23 depends on Claim 13, therefore including the problematic "when" element, and adds additional limitations regarding a first and second FIFO and certain interpolation circuitry contained in the video pipeline. The first FIFO receives a first stream of words of data from the frame buffer, and the second FIFO receives a second stream of words of data from the frame buffer. The meaning of FIFO is set forth above, in connection with Claim 16. This claim further teaches that the second FIFO is "disposed in parallel" with the first FIFO.

ATI argues that "disposed in parallel" means the FIFOs must be "positioned in parallel with the video pipeline", and "sharing circuitry". ATI then insists that this limitation "precludes coverage of only a single memory structure". Cirrus, on the other hand, asserts that under this claim, the two FIFOs are part of the video backend pipeline, and must be parallel with each other. Cirrus also contradicts ATI's assertion that a single memory structure could not come within this claim, and instead argues that a single memory structure may be internally segmented to operate as two independent FIFOs, which would fall within the claim language. The Staff takes no position on any of the claim construction issues associated with Claim 23.

The plain language of Claim 23 supports Cirrus' position with regard to "disposed in parallel" as the claim language makes clear that one FIFO is parallel to the other FIFO. The parties' arguments regarding the single memory structure pertain to the infringement issue, and will be addressed in that portion of the initial determination. No dispute exists among the parties regarding the meaning of the "interpolation circuitry" limitation of Claim 23, which teaches circuitry to generate, from the first and second streams of data in the FIFOs, additional pixel data through an averaging or estimating process.

B. Whether ATI's Rage Devices Infringe the Inserted Claims

Cirrus asserts that it has demonstrated by a preponderance of the evidence that every limitation of Claims 13, 15, 16, 17, 23 and 37 of the '525 Patent are found in ATI's Rage Devices. ATI contends that its accused products do not infringe these claims, while the Staff similarly argues that Cirrus has not established by a preponderance of the evidence that the ATI Rage Devices fall within the scope of independent Claims 13 or 37 of the '525 Patent or dependent Claims 15, 16, 17 or 23. The Staff, however, distinguishes the ATI Rage Devices from the asserted claims based only on the "when" limitation of Claim 13 and the "multi-format frame buffer" requirement in Claim 37, and takes no position on the other infringement-related disputes between ATI and Cirrus. Although I have already concluded that the "when" limitation of Claim 13 renders that claim, and its dependents, Claims 15, 16, 17 and 23 invalid for indefiniteness, and the "fourth mode" limitation of Claim 15 also renders that claim indefinite, I address in turn, where possible, whether the ATI Rage Devices meet the other limitations of those claims as well as the limitations of Claim 37.

1. Claims 13 and 37

a. Whether the ATI Rage Devices are "Controllers" or "Display" Controllers" within the Meaning of Claims 13 and 37

Cirrus contends that the accused products, the ATI Rage Devices, contain only a single controller, are highly integrated, rather than modular designs, and are implemented on a single integrated circuit, thereby meeting the single controller "integrated design" limitation that Cirrus proposed with respect to claim construction. ATI argues that Cirrus' desired construction is an attempt to distinguish prior art that does not constitute a single integrated

design, that no such limitation exists in Claims 13 and 37, but that even if there were such a limitation, its products would not infringe as they are intentionally designed as modular systems.

In construing the term "a controller", I have concluded that it covers not only a unitary integrated design, but also a modular component design. Inasmuch as the term encompasses both types of designs, and ATI essentially concedes that its products escape infringement of this limitation only if I adopted Cirrus "single, non-modular design", I find that the ATI Rage Devices satisfy this element of Claims 13 and 37.

b. Whether The ATI Rage Devices Contain Circuitry for Selectively Writing Data into On-Screen and Off-Screen Memory Of A Frame Buffer

As to the "circuitry for selectively writing" element of this claim limitation, ATI argues that the ATI Rage Devices do not satisfy it because [

] ATI Post-Hearing Brief at 27. Based on my construction of "circuitry for selectively writing", *supra*, as referring to the writing of data into one or the other of the memory regions, the ATI Rage Devices have this claim element by ATI's own admission. Mr. Bicevskis' testimony, Tr. at 277-78 and 284-85 support this finding, as does Mr. Ferraro's expert opinion, Tr. at 508-09.

Turning to the "frame buffer" element, Cirrus alleges that if properly construed, Claims 13 and 37 each require a frame buffer that is divided into on-screen and off-screen regions and that holds video and graphics data in their native formats. Cirrus further alleges that the ATI Rage Devices have exactly this type of frame buffer. ATI responds that a proper construction

of these claims requires an undifferentiated memory that does not divide video and graphics into separate regions and that because the ATI Rage Products [

] there is no infringement of either Claim 13 or 37. ATI further argues that even if the Staff's proposed construction is adopted, which distinguishes Claim 37's multi-format frame buffer, requiring the capability to store simultaneously both graphics *and* video in each region, from Claim 13's frame buffer, which merely must be able to store graphics *or* video in each region, the accused devices still would not infringe Claim 13 because [

]

In construing Claims 13 and 37, I have concluded that a distinction does exist between the frame buffer limitation of Claim 13 and the multi-format frame buffer limitation of Claim 37 and have found that the specification supports the conclusion that the frame buffer of Claim 13 must be able to store video *or* graphics data in each region while the multi-format frame buffer of Claim 37 requires the capability to store simultaneously both video *and* graphics data in each region. Inasmuch as Cirrus admits, CFF 498, and the record supports, Bicevskis, Tr. at 1120, that the ATI Rage Devices [ ] I conclude that they do not contain either the "frame buffer" of Claim 13 or the "multi-format frame buffer" of Claim 37 and therefore do not satisfy the "frame buffer"/"multi-format frame buffer" limitations of these claims.

c. Whether the ATI Rage Devices Contain the "First Port" Limitation of Claim 13

ATI argues that the ATI Rage Devices do not meet the limitation of Claim 13 setting

forth the "first port for receiving video and graphics data ..." on the grounds that this limitation requires the input port to have the capacity to recognize words of data as either graphics or video in order to direct its processing in the appropriate set of frontend processing circuitry prior to the data being stored in display memory. As I concluded in the claim construction section, the "first port" described in Claim 13 requires the interface to have the ability to decode the addresses accompanying the data so as to recognize the data as video or graphics in order to forward it to the appropriate frontend processing circuitry. [

] This aspect of the ATI Rage Devices was confirmed by Mr. Bicevskis. Bicevskis, Tr. at 282-86, 1130-31, 1200-01.

Cirrus argues that [

] thus satisfying the requirements of this limitation of Claim 13. ATI asserts, however, that [

]

As Cirrus correctly noted in its Post-Hearing Brief at 50, "[t]he infringement issue here turns on the claim interpretation issue ...." Having accepted ATI's proposed construction of the "first port" limitation in the '525 Patent as requiring some recognition of data as graphics or video, and some frontend processing, and considering that Cirrus does not present any credible evidence disputing the description of the ATI Rage Devices' host bus interface testified to by Mr. Bicevskis, I conclude that the ATI Rage Devices do not meet the "first port" limitation of Claim 13.

d. Whether the ATI Rage Devices Contain the "Second Port" Limitation of Claim 13

Cirrus asserts that the ATI Rage Devices meet Claim 13's requirement of a second port for receiving real-time video data, and relies on Dr. Peuto's testimony for support. ATI does not dispute, either in its briefs or its response to Cirrus' Proposed Findings of Fact, the existence of this claim element in its accused products.

e. Whether the ATI Rage Devices Meet the "Circuitry for Generating an Address" Limitation of Claim 13

Cirrus asserts that this claim limitation is met in the ATI Rage Devices, and argues Dr. Peuto's acknowledgment thereof, as well as noting Mr. Ferraro's affirmative opinion to that effect. While ATI fails to address infringement of this claim limitation in its briefs, in its responses to Cirrus' Proposed Findings of Fact, ATI raises a challenge on this issue based on the involvement of the CPU in generating addresses, as expressed by ATI's Mr. Bicevskis. In response to questioning on this topic, Mr. Bicevskis initially failed to offer a clear explanation as to the existence of circuitry for generating an address and its relationship to the CPU. Ultimately, however, upon further questioning, Mr. Bicevskis agreed that [

] Bicevskis, Tr. at 295-96. Cirrus' expert, Mr. Ferraro, also offered an affirmative opinion as to the [ ] and his explanation of its functioning in relation to the CPU reflected a reasonable consistency with Mr. Bicevskis' explanation of the functioning. Ferraro, Tr. at 520-21. Additionally, I note that ATI did not dispute Cirrus' Proposed Finding of Fact, CFF 539, that Mr. Li testified [ ] JX 13C at 61. Accordingly, I conclude that Cirrus has met its burden of showing that the ATI Rage Devices satisfy this claim limitation.

f. Whether the ATI Rage Devices Meet the "Circuitry for Selectively Retrieving" Limitations of Claims 13 and 37

With regard to the limitations of Claims 13 and 37 concerning circuitry for selectively retrieving, Cirrus asserts that the ATI Rage Devices have selective retrieval circuitry, noting that Mr. Bicevskis [ ] Bicevskis, Tr. at 296-97. While I rejected Cirrus' proposed interpretation of this claim language, I do find that Mr. Bicevskis' testimony regarding the ATI Rage Devices reflects that [ ] Bicevskis, Tr. at 296-99. As to the "as ... rastered" portion of Claim 13's "circuitry for selectively retrieving" limitation, Cirrus maintains the ATI Rage Devices do this, and relies for support on Mr. Bicevskis' testimony that [ ] Bicevskis, Tr. at 301-02. ATI contends that Cirrus' evidence does not establish that both graphics and video are

retrieved, as[

]

I previously rejected ATI's indefiniteness arguments as to these claim limitations, and based on the testimony of Mr. Bicevskis, particularly Tr. at 296-302, 1000-001, and 1200, I conclude that the ATI Rage Devices meet the "circuitry for selectively retrieving" limitations of both Claim 13 and Claim 37[17], including Claim 13's requirement that the selective retrieval occur "as data is rastered for driving a display." ATI's argument that the "data" being retrieved must be the very same data being displayed finds no support in the '525 Patent and defies engineering reality in light of the previously discussed delays inherent in data retrieval and processing. Mr. Bicevskis displayed an ability to sufficiently understand and apply the terms used in these claim elements, and his explanation of the ATI Rage Devices adequately demonstrates their satisfaction of these claim requirements, as I have construed them.[18]

g. Whether the ATI Rage Devices Satisfy the "Graphics Backend Pipeline"/"First Pipeline" and the "Video Backend Pipeline"/"Second Pipeline" Elements of Claims 13 and 37

I previously found that Claim 37's "first pipeline" is a backend pipeline, thus resolving the dispute between ATI and Cirrus on that claim limitation. The parties agree that the ATI

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[17]Although the portion of Claim 37 in question also includes a reference to the multi-format frame buffer previously found to be lacking in the ATI Rage Devices, I will not revisit that issue in connection with this claim limitation of Claim 37.

[18]While Cirrus' expert, Mr. Ferraro, also gave an opinion that these limitations are satisfied by the ATI Rage Devices, Mr. Ferraro relied on what he characterized as an [

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Rage Devices contain a graphics backend pipeline and a video backend pipeline. However, although ATI makes no argument on this issue in its briefs, and having never raised this argument before, ATI, in response to Cirrus' Proposed Findings of Fact, contends that Cirrus failed to show that the graphics pipeline in the accused devices is completely separate and distinct from the video pipeline, as required by Claims 13 and 37. In response to questioning by Cirrus, Mr. Bicevskis testified that [

] See Bicevskis, Tr. at 302-04.

Notably, however, ATI's own Dr. Peuto not only explicitly testified that [

] See Peuto, Tr. at 1341-42, 1347. Even given that ATI took the position that these claim limitations allow for the sharing of circuitry, Cirrus' contrary position was well known to ATI and to Dr. Peuto in light of ATI's earlier motion for summary determination as to the invalidity of Claim 37 based on the Parallax 1280/Viper, which brought the shared circuitry question to the forefront. Under the circumstances, therefore, Dr. Peuto's unqualified testimony that [ ] given the absence of any evidence or even affirmative assertion by ATI to the contrary, adequately satisfies Cirrus' burden of establishing these claim elements.

h. Whether the ATI Rage Devices Have "Circuitry for Retrieving Always Rastering a Stream of Data from Said Frame Buffer to Said Graphics Backend Pipeline"

Cirrus and ATI generally agree on the functioning of the circuitry for retrieving found

in the ATI Rage Devices, but, as set forth in the earlier section on claim construction, disagree on whether the ATI Rage Devices meet this limitation of Claim 13. Cirrus convincingly argues that all the elements ATI highlights as distinguishing the ATI Rage Devices from what is set forth in the '525 Patent on this point are actually described in the specification of the '525 Patent. Applying the proper construction of the "always rastering" limitation, which allows for engineering delays in the retrieval of data, the ATI Rage Devices contain this circuitry as described in Claim 13. While the circuitry in the ATI Rage Devices [

] See Bicevskis, Tr. at 306-07.

i. Whether the ATI Rage Devices Have "Circuitry for Retrieving ... Rastering Video Data to Said Video Backend Pipeline When a Display Raster Scan Reaches a Display Position of a Window"

As set forth, *supra*, in the claim construction section, the "when" limitation of Claim 13 is invalid for indefiniteness, and therefore cannot be applied against the ATI Rage Devices to make an infringement determination. While Cirrus argues that the ATI Rage Devices meet this claim limitation because "[t]he position of the raster scan is a factor in the video retrieval algorithm" and "[t]here is a variable temporal relationship" between the rastering of data to the video backend pipeline and the display of video in the display window (See CFF 563, 564), this argument shows the indefinite nature of this claim limitation. Additionally, although ATI and Cirrus agree that the ATI Rage Devices [

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] Because

neither the '525 Patent nor expert testimony based on the understanding of one ordinarily skilled in the art conclusively establish the range covered by "when", there is no measure by which to compare the ATI Rage Devices to this claim limitation.

j. Whether the ATI Rage Devices Contain the "Output Selector Circuitry" Set Forth in Claim 13

Cirrus relies on the testimony both of Dr. Peuto and Mr. Ferraro as evidence of the existence in the ATI Rage Devices of the output selector circuitry limitation of Claim 13 of the '525 Patent. ATI raises no objection to this assertion, either in its briefs or its responses to Cirrus' Proposed Findings of Fact. I find that the ATI Rage Devices satisfy the "output selector circuitry" limitation of Claim 13. See Peuto, Tr. at 1354; Ferraro, Tr. at 556.

2. Claim 15

While Cirrus argues that all the limitations of Claim 15 are met by the ATI Rage Devices, ATI buttresses its invalidity argument with an argument that even assuming, *arguendo*, the definiteness of this claim, several claim requirements are missing.

I have concluded, *supra*, that even apart from its invalidity and noninfringement due to dependence on Claim 13, the additional, independent portion of Claim 15, in particular the "fourth mode" limitation, fails to meet the requisite level of definiteness mandated by Section 112, 35 U.S.C. § 112, resulting in a further finding of invalidity. Due to the indefinite

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[19]Dr. Peuto indicated that [

] Peuto, Tr. at 1547.

nature of the claim, it cannot be applied to the ATI Rage Devices in order to make an infringement determination.

3. Claims 16, 17 and 23

Although the dependency of Claims 16, 17 and 23 on Claim 13, found to be both invalid and not infringed, renders moot a separate analysis of the infringement of these claims, such a separate analysis is undertaken here ignoring, *arguendo*, the noninfringement and invalidity based on Claim 13. With regard to Claims 16, 17 and 23, all of which reference the existence of a first and second FIFO, ATI and Cirrus agree that the ATI Rage Devices do not literally infringe because they lack FIFOs, [ ] Cirrus argues, however, that the ATI Rage Devices infringe Claims 16, 17 and 23 under the Doctrine of Equivalents. Cirrus asserts that the ATI Rage Devices' [ ] are "substitute element[s]" that are the substantial equivalents of the FIFOs disclosed in Claims 16 and 23. ATI disagrees with Cirrus both as to the facts and the law. Tacitly conceding that all other claim elements are met, ATI contends that the ATI Rage Devices have [ ] such that in an element-by-element equivalency comparison, no corresponding element exists for both the first *and* the second FIFO, and further contends that the [ ] is not equivalent to the dual FIFOs of the '525 Patent.

As the Supreme Court recently stated in Warner Jenkinson Co. v. Hilton Davis Chemical Co., 520 U.S. 17, 40 (1997), "[a]n analysis of the role played by each element in the context of the specific patent claim will thus inform the inquiry as to whether a substitute element matches the function, way, and result of the claimed element, or whether the substitute element plays a role substantially different from the claimed element." The role played by the

dual FIFOs can best be understood both by considering the meaning of FIFO to one of ordinary skill in the art, and by looking to the description of the FIFOs' function in Claims 16 and 23. As indicated in the claim construction section, *supra*, and as agreed by the parties, a FIFO is understood by those of ordinary skill in the art to be a memory space where data is read out in the same order it was written in. Claim 16 teaches that in the video pipeline, the first FIFO receives a plurality of words of data "for" a first display line of pixels in memory, and the second FIFO receives a plurality of words of data "from" a second display line of pixels in memory. Claim 23 discloses that in the video pipeline, the first FIFO receives a first stream of words of data from the frame buffer, the second FIFO, disposed in parallel to the first, receives a second stream of words of data from the frame buffer, and interpolation circuitry uses the output from each of the FIFOs to generate additional data for scaling purposes.

As a threshold matter, I do not find persuasive ATI's argument regarding the impossibility of one structure, [ ] serving as an equivalent for two structures, the dual FIFOs. Although ATI correctly notes that the proper analysis focuses on an element-specific comparison, this serves to guard against "allowing the concept of equivalence to eliminate completely" the requirement of finding some identical or equivalent structure for each claimed element in the patent. See Warner-Jenkinson, 520 U.S. at 40. This analysis does not preclude the possibility that one structure, [ ] *could* be the equivalent of two claimed elements, such as the first FIFO and the second FIFO, so long as it meets the equivalency test for each in the context of their roles in each claim. Accordingly, in light of this, and in light of the lack of dispute as to the functionality of the [ ] I

conclude that it is not necessary to resolve the factual dispute between ATI and Cirrus regarding whether the ATI Rage Devices have [ ]

For its equivalency argument, Cirrus maintains that ATI's [ ] performs the same function as the FIFOs, in that the [ ] serves as a delay element to accept and hold data from a first and second line, in order to allow for simultaneous extraction for interpolation. Next, Cirrus asserts that the [ ] performs this function in the same way as the FIFOs, by accepting and storing video data from left to right for one line, then left to right for the next line, and by outputting that as one pixel from the first line and one pixel from the second line, in order from left to right. As to the result, Cirrus argues the [ ] achieves the same result of providing vertically adjacent pixels to the vertical interpolator in the ATI Rage Devices.

While ATI essentially seems not to dispute Cirrus' characterization of the function and the result of the [ ] with respect to vertical interpolation, ATI insists that the *way* the [ ] operates is not equivalent to the way the dual FIFOs of the '525 Patent operate. According to ATI's Oswin Hall, an engineering design leader for the ATI Rage Devices, the [

] Hall, JX 8C at 89-99. Mr. Hall also testified that he was the indirect source of information on this issue for ATI's expert, Dr. Peuto. Hall, JX 8C at 91-92. ATI argues, as a result, that [

] and so operates in a different way than the dual FIFOs. ATI also notes that [

] is significantly different than in the dual FIFOs. Cirrus acknowledges that the [

] Cirrus' Comment on RFF 448-449. However, Cirrus maintains that, the *way* is substantially the same, and the reordering is an unimportant distinction because the data is read out in a way that does not disrupt the order it was read in from the standpoint of how it is to be displayed on the screen.

Whether this acknowledged difference in the *way* the [ ] functions from the *way* the two FIFOs function is a substantial difference should be determined with consideration of the view of one ordinarily skilled in the art. See Texas Instruments, Inc. v. U.S. Int'l Trade Comm'n, 805 F.2d 1558, 1562 (Fed. Cir. 1986) (noting that same analytical framework for determining scope of claims applies in the context of alleged infringement under doctrine of equivalents). Accordingly, turning to the expert testimony offered on this issue, Cirrus' expert Mr. Ferraro testified as one skilled in the art that the [ ] constitutes an equivalent both to the first FIFO and to the second FIFO, and offered a credible and convincing explanation for his opinion, incorporating an apparent understanding of the functioning of the [ ] consistent with Mr. Hall's testimony regarding its functioning. Ferraro, Tr. at 672-89. ATI's technical expert, Dr. Peuto, offered a contrary opinion as to equivalency, but his statements regarding the functionality of the [ ] the ATI Rage Devices are inconsistent with Mr. Hall's. The relevant excerpt of Dr. Peuto's testimony follows:

[

]

Peuto, Tr. at 1359-60 (emphasis added).

Given that Dr. Peuto's stated understanding of the [ ]' functionality differed markedly from that of Mr. Hall, who, by his own admission was the likely source of Dr. Peuto's underlying information, I cannot rely on Dr. Peuto's opinion on this equivalency issue.

Therefore, because Mr. Ferraro's testimony constitutes the only credible expert evidence of record on this issue and his testimony indicates that one skilled in the art would consider insubstantial and unimportant the difference in the way the [ ] operates from the way the FIFOs operate, I find that Cirrus has met its burden of proof to establish the [ ] as the equivalent of the dual FIFOs described in Claims 16, 17 and 23 of the '525 Patent. Because the ATI Rage Devices contain this equivalent, and ATI raises no other arguments that the ATI Rage Devices do not satisfy other limitations of Claims 16, 17 and 23, assuming, *arguendo*, the validity of these claims, and ignoring the noninfringement of these claims based on the absence of elements required by Claim 13, they would otherwise be

infringed by the ATI Rage Devices.

III. Validity

A. On-Sale Bar

Under 35 U.S.C. § 102(b), a patent is invalid if "...the invention was ... on sale in this country, more than one year prior to the date of the application for patent in the United States". This invalidity ground is often referred to as the "on-sale bar". The on-sale bar applies where a commercial offer for sale of the patented article occurred more than one year before the patent application date, at a time when the invention was ready for patenting. Pfaff v. Wells Elec., Inc., 119 S.Ct. 304, 311 (1998). The invention may be deemed ready for patenting even though not reduced to practice if the inventor had, at that time, created sufficiently specific drawings or a description of the invention to enable a person skilled in the art to practice the invention. Id. at 312. Thus, the existence of an operable device need not be established as a prerequisite for application of the on-sale bar. See, e.g., C.R. Bard, Inc. v. M3 Systems, Inc., 157 F.3d 1340, petition for rehearing denied, 161 F.3d 1380 (Fed. Cir. 1998); Barmag Barmer Maschinenfabrik AG v. Murata Machinery, Ltd., 731 F.2d 831, 837 (Fed. Cir. 1984). Operability should be considered only to the extent it demonstrates that a claimed element of the invention had not yet been invented, or the inventors did not know they had a workable invention and thus had nothing to offer for sale. See, e.g., C.R. Bard, Inc., 157 F.3d at 1358; Petrolite Corp. v. Baker Hughes, Inc., 96 F.3d 1423, 1427 (Fed. Cir. 1996) ("[T]he thrust of the on-sale inquiry is whether the inventor thought he had a product which could be and was offered to customers, not whether he could prevail under the technicalities of reduction to practice . . . ." (quoting Paragon Podiatry Lab., Inc. v. KLM Lab., Inc., 984

F.2d 1182, 1187 n.5, 25 USPQ2d 1561, 1570 n.5 (Fed. Cir. 1993)).

ATI argues that the offers by Cirrus to sell its CL-GD7542 Nordic product ("Nordic product") prior to January 23, 1994 (one year before the '525 Patent application date) invalidate the '525 Patent under the on-sale bar. Because of previous discovery misconduct by Cirrus, I entered a rebuttable, adverse factual inference against it in Order No. 47, that the Nordic product was on sale before January 23, 1994. In light of Cirrus' April 27, 1999 Notification and Declaration, and the proffered stipulation made therein, as set forth above, it is conclusively established that Cirrus offered the Nordic product for sale in the United States prior to January 23, 1994.

Prior to the stipulation, in support of its on-sale argument, ATI contended that while the record does not reflect evidence that an actual sale of the Nordic product occurred prior to the critical date,[20] no actual sale is necessary for application of the on-sale bar. ATI relied in part on U.S. promotion efforts for the Nordic to establish that the product was offered for sale. While Cirrus had previously taken the position that the Nordic product was not ready for patenting, ATI asserted otherwise. Although ATI acknowledged that no evidence established that the Nordic product had been reduced to practice before the critical data, ATI took the position that the invention was sufficiently specifically described in drawings and other descriptions to enable one skilled in the art to practice it.

With regard to whether the Nordic product practiced the asserted claims of the '525 Patent, ATI argues that all claim elements of Claims 13 and 37 were met, and that Claims 15,

[20] ATI did suggest that pre-critical date sales of the Nordic product must have occurred between Cirrus Logic International, and its wholly owned subsidiary, Cirrus Logic KK. However, ATI pointed to no direct evidence of such sales.

16, 17 and 23 were obvious in light of the Nordic product in combination with other prior art references. Cirrus, on the other hand, raises no technical arguments against anticipation of Claim 37, but contends that ATI has not met its burden of showing that all Claim 13 elements were present in the Nordic product, and has failed to establish obviousness for the other claims. Cirrus first argues the impropriety of ATI's reliance on an undated technical specification as outlining the Nordic product allegedly offered for sale.

The "when" limitation from Claim 13 and the indefinite "fourth mode" limitation of Claim 15 render it impossible to apply those claims to a device, because no determination can be made regarding the satisfaction of such indefinite claim limitations. Nonetheless, technical arguments relating to other limitations will be considered. Cirrus takes the position that the Nordic product did not anticipate the "always rastering" and the "second port" for video/"address-generation circuitry" elements. With regard to the video port, the parties agree that the Nordic product that was ultimately sold did not include that feature, but ATI argues that the product design offered for sale at an earlier date contained a video port. Those previous elements also apply to Claim 15, dependent on Claim 13, and Cirrus also alleges a lack of evidence that the Nordic product practiced the color key system in the third and fourth modes of Claim 15. While ATI admits that the color key element was missing from the Nordic product, ATI maintains it would have been obvious to combine this feature with the Nordic product. Similarly, while the Nordic design did not feature interpolation using dual FIFOs, as described in Claims 16, 17 and 23, ATI argues the obviousness of combining such a feature with the Nordic product.

The Staff contends that the Nordic product was ready for patenting on or before the

critical date, and that the Nordic product meets all but one of the elements of Claim 13. Specifically, the Staff argues that the Nordic product did not meet the "when" limitation of Claim 13, and that therefore no clear and convincing evidence supports a finding that the Nordic product practiced Claim 13 as properly construed.

Even apart from Cirrus' stipulation, based on the evidence in the record and on Cirrus' failure to rebut the adverse factual inference previously entered against it, I would otherwise conclude that Cirrus placed the Nordic product on sale prior to the critical date. However, I find that the Nordic product violated the on-sale bar under Section 102(b) only as to Claim 37, as the Nordic product did not practice the other asserted claims of the '525 Patent, and/or those claims have been deemed invalid.

The stipulation by Cirrus is consistent with the evidence. Despite the prior rebuttable factual inference that the Nordic product was on sale in the U.S. prior to the critical date, I note that Cirrus never offered any direct evidence or testimony to squarely refute this. Although Cirrus offered an overview of the marketing and sales of the Nordic product through Robert Dickinson, Cirrus never elicited a direct statement that the product was not offered for sale in the U.S. prior to the critical date. Instead, the closest Mr. Dickinson came was testifying that [

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In fact, however, his understanding in this regard does not correspond to the law surrounding offer for sale, as a reduction to practice is not required. Although his testimony seemed designed to cast doubt that such offers for sale occurred, given the factual inference, Cirrus was obliged to offer more.

The totality of the circumstances reflects that, regardless of the stipulation, the Nordic product was on sale in the U.S. prior to January 23, 1994. In 1993, Cirrus [

]

Although clearly the Nordic product was not physically available, or reduced to practice in very early 1994, such an occurrence is not required for application of the on-sale bar, and, even apart from the stipulation, the record reflects that the Nordic product was ready for patenting. See Pfaff, 119 S.Ct. at 309. Cirrus has admitted that the major function specification, describing the features and capabilities of the Nordic, closed in [

] Cirrus also apparently had a high enough degree of confidence in the operability and feasibility of the Nordic product design to promote the Nordic product to its most valuable customers. In addition, evidence in the record shows that Cirrus engaged in [

] Although not offers to sell *in the U.S.*, this evidence indicates Cirrus' confidence in the Nordic product and its substantial design completion at that

point in time. Even had Cirrus faced subsequent "design difficulties" in producing the Nordic product, as it claims, application of the on-sale bar does not require that the inventor have been able to "prevail under the technicalities of reduction to practice." See Petrolite, 96 F.3d at 1427. Mr. Dickinson made clear that [

]

Turning to Cirrus' argument that even if on sale prior to the critical date, the Nordic product did not practice the '525 Patent, and so should not trigger the on-sale bar, I conclude that the record supports a finding that of the asserted claims, the Nordic product practiced only Claim 37. No party disputes that the Nordic product practiced Claim 37, and therefore I find that the on-sale bar invalidates this claim. As to the practice of Claim 13, which the parties disputed, the only claim elements in contention are the video port and "always rastering" limitations. While the "when" limitation invalidates Claim 13 and its dependent claims, and Claim 15 has also been deemed invalid on other grounds, I additionally find the "always rastering" element is missing from the Nordic product, such that it did not practice this claim or its dependents, regardless of the invalidity ruling.

Turning first to the video port element, the record reflects that [

]

ATI, however, failed to meet its burden of showing that the Nordic product met the

"always rastering" element of Claim 13. ATI relied on testimony by its expert, by Cirrus employee [ ] and on the Nordic technical specification in support of its position as to this limitation. Based on my review of the cited evidence, I find it inconclusive and/or unpersuasive on this issue, and therefore must find that ATI failed to carry its burden of clear and convincing proof on this point. In the deposition passage of [ ] the witness seemed to misunderstand the questioning on this issue, to lack the necessary knowledge to respond, or to provide nonresponsive answers. Similarly, the Nordic specification lacks clarity on this point, as both ATI and Cirrus argue it supports their contrary positions, and neither offered adequate expert testimony to clarify the allegedly relevant portions of the specification. Additionally, ATI's expert testimony from Dr. Peuto reflected a lack of substantiation for or explanation of his position. Accordingly, placing aside indefiniteness, and finding this "always rastering" claim limitation lacking, this ground of invalidity must be rejected as to Claim 13, as ATI has not demonstrated that Cirrus' offer for sale of the Nordic product triggered the on-sale bar for this claim, and the obviousness defense as to dependent Claims 15, 16, 17 and 23 must also be rejected, as ATI made no obviousness argument as to this missing element and therefore failed to establish that the sale of the Nordic product, in combination with other prior art, rendered these claims obvious. Accordingly, Claim 37 is invalid due to the on-sale bar, but the on-sale bar does not invalidate the other asserted claims.

B. Section 102(b) - Anticipation

35 U.S.C. § 102(b) provides that no entitlement to a patent exists where:

> the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application

for patent in the United States ...

A prior art reference in a printed publication triggers invalidity by anticipation if it discloses each and every limitation of the patent claim, either explicitly or inherently. Hazani v. U.S. Int'l Trade Comm'n, 126 F.3d 1473, 1477 (Fed. Cir. 1997); see also In re Graves, 69 F.3d 1147, 1152 (Fed. Cir.), cert. denied, 517 U.S. 1124 (1996) (allowing for anticipation even where disclosure is not explicit, if the feature would be within the knowledge of one skilled in the art). The "printed publication" of Section 102(b) must have been accessible to the public, and must sufficiently describe the invention so as to enable one skilled in the art to reduce it to practice. See Carella v. Starlight Archery & Pro Line Co., 804 F.2d 135, 139 (Fed. Cir. 1986) (concerning public availability); In re Spada, 911 F.2d 705, 708 (Fed. Cir. 1990) (noting requirement for sufficiency of description of invention).

ATI argues anticipation of claims of the '525 Patent by three prior art references: (1) Oak Technology, Inc.'s ("Oak") Spitfire OTI-64107 chip in connection with Brooktree Corporation's ("Brooktree") Bt885 chip and other associated circuitry (collectively, "Oak/Brooktree"); (2) Intel Corporation's ("Intel") i750 product, which includes the 82750 Display Processor, the 82750 Pixel Processor, and video digitizer circuitry (collectively, "Intel i750); and (3) Parallax Graphics, Inc.'s Parallax 1280 and VIPER products (collectively, "Parallax 1280/Viper"). Although my ruling regarding the indefiniteness of the "when" limitation of Claim 13 and the "fourth mode" limitation of Claim 15 renders Claims 13, 15, 16, 17 and 23 invalid, and although the on-sale bar renders Claim 37 invalid, the anticipation defense will be separately considered to the extent possible.

1. Oak/Brooktree

The Oak Spitfire was designed to interface with Brooktree's Bt885, but the devices were separate chips, and were sold as separate products. ATI takes the position that Claims 13, 15 and 37 are directly anticipated by the Oak Spitfire as it interfaced with the Bt885 ("Oak/Brooktree"), while Claims 16, 17 and 23 are obvious in view of Oak/Brooktree in combination with other prior art. ATI relies on the testimony of Jonathan Siann, the Bt885 architect who also helped design the Oak Spitfire, and the deposition testimony of Tuan Nguyen, Oak Spitfire project manager, as well as on various documents, to establish the Oak/Brooktree as invalidating prior art. Cirrus counters that ATI improperly attempts to assert the Oak/Brooktree, a combination of references, for anticipation, which requires a single reference. Cirrus also disputes the status of Oak's product as prior art. Furthermore, Cirrus contends that the Oak/Brooktree fails to meet several limitations of the asserted claims. The Staff makes no statement regarding its view on the issue of prior art status, but indicates that no clear and convincing evidence establishes anticipation of Claim 13 or Claim 15 by Oak/Brooktree.

As to the status of the Oak/Brooktree combination as prior art, Cirrus insists that these separate products sold by separate companies cannot be combined for anticipation purposes. ATI argues that the Bt885 product was intended to form only part of a complete display controller architecture, such that its combination with and/or incorporation into other products such as the Oak Spitfire was expected, and was discussed in printed publications such as the June 1993 article in Electronic Design magazine and the July 5, 1993 article in Electronic Engineering Times. ATI specifically states that the Electronic Design article included a drawing and discussion that disclosed all the requisite features of the overall Oak/Brooktree

architecture. In light of the rulings set forth below, I deem it unnecessary to resolve whether the Oak/Brooktree combination can be considered a single prior art reference, but will assume, *arguendo*, for purposes of the ensuing discussion, that the combination may be regarded as a single reference.

As to the disclosure in the articles, Cirrus responds that neither of these news articles sufficiently describes the product so as to satisfy the enablement requirement of a Section 102(b) printed publication. ATI also contends that Oak's January 14, 1994 specification for the Oak product, or a non-confidential slide presentation at a conference by Mr. Siann in March 1993 could also serve as anticipatory printed publications. As to the specification, Cirrus indicates that no satisfactory evidence shows that this was publicly released absent a non-disclosure agreement, while ATI cites testimony by Mr. Nguyen that it was likely available to the public, and Cirrus further argues that no evidence establishes that the specification meets the enablement requirement. As to the status of Mr. Siann's slide presentation as prior art, Cirrus claims that it was a high-level presentation that did not disclose a complete display controller architecture.

Turning first to the publications ATI cites as prior art under Section 102(a) and Section 102(b), I conclude that ATI has not met its burden to establish by clear and convincing evidence these documents as invalidating prior art. The Oak specifications and technical documents cannot qualify as prior art because no clear and convincing evidence establishes their non-secret, public availability prior to January 23, 1994. See Carella v. Starlight Archery & Pro Line Co., 804 F.2d at 139. Mr. Nguyen, the Oak/Spitfire project manager, testified that he could not recall any specifics regarding when the product specifications would have

been publicly disclosed, and further could not recall whether the disclosure of these specifications was only made under a non-disclosure agreement, as was Oak's general practice. ATI offered no other testimony on this point. The mere dates on the faces of these documents are not enough to indicate their disclosure on those dates, and even assuming, *arguendo,* they were disclosed prior to the critical date, uncertainty remains regarding whether this would have happened in the context of a non-disclosure agreement, so as to avoid triggering prior art status.

The two articles and the slide presentation cited by ATI as prior art publications, although published more than one year prior to the date of application for the '525 Patent, cannot qualify as invalidating prior art because ATI has failed to meet its burden of proving that they meet the enablement requirement. See In re Spada, 911 F.2d at 708 (holding that in order to anticipate, "the [prior art] reference must describe the applicant's claimed invention sufficiently to have placed a person of ordinary skill in the field of the invention in possession of it"). ATI offers little evidence or argument on the enablement issue as to the slide presentation or the Electronic Design and Electronic Engineering Times articles, failing to point to any expert testimony from the perspective of one skilled in the art, and instead merely asserting that the slides and the articles reveal the relevant architecture. While some testimony from Mr. Siann and Mr. Nguyen regarding the disclosure in the articles and the slides is included in the record, this does not constitute expert testimony, and is also problematic because the testimony comes from persons involved in the design of the products at issue, such that they likely have an extraordinary level of knowledge of and direct experience with the products themselves. Cirrus asserts that the articles just contain high-level feature descriptions

that cannot satisfy the enablement requirement. Based on my review of the record, I must conclude that ATI failed to meet its burden of establishing these articles and the slide presentation as enabling, and they therefore cannot qualify as anticipatory prior art.

Finally, ATI claims that the Oak Spitfire itself, as it interfaced with the Bt885 architecture, was on sale in the United States prior to January 23, 1994, such that it constitutes Section 102(b) prior art. Cirrus responds that the only evidence in the record concerning the sale date of the Oak Spitfire consists of the two magazine articles inaccurately predicting its available date, and fails to satisfy ATI's burden on this point. Mr. Nguyen testified only that he believed the Oak Spitfire was not produced until early 1994. JX 2C at 24.

Cirrus also claims that the actual invention date of the '525 Patent was in September 1993, entitling it to an earlier priority date, but ATI denies that Cirrus met its burden in establishing the earlier date. The Federal Circuit's decision in Mahurkar v. C.R. Bard, Inc., 79 F.3d 1572, 1576 (Fed. Cir. 1996) notes that a patent challenger, in this case ATI, always continues to bear the burden of persuasion on its invalidity challenge, including on sub-issues such as prior art status. When a party asserts an invention date prior to the patent filing date, that party bears the burden of production of evidence showing the earlier invention date. Id. The Mahurkar court also notes the long-standing rule that a party seeking to show conception through the oral testimony of an inventor must also provide corroborating evidence, such that more than just inventor testimony must be offered. Id. Given the production of evidence of the earlier invention date, the burden of proof by clear and convincing evidence continues to rest with the patent challenger. Id.; see also Innovative Scuba Concepts, Inc. v. Feder Ind., Inc., 26 F.3d 1112, 1115 (Fed. Cir. 1994) (holding that district court erred in placing on the

patentee the burden of proving an invention date earlier than its filing date to overcome invalidity based on prior art, and stating that "...the presumption of validity remains intact and the ultimate burden of proving invalidity remains with the challenger throughout the litigation").

In support of the earlier invention date, Cirrus points to testimony by the inventors, Mr. Nally and Mr. Schafer, regarding their fall 1993 conception of the invention and their subsequent diligent efforts to reduce the invention to practice and patent it. As corroborating evidence, Cirrus offers the inventors' architectural proposal documents from October and November 1993, with the acknowledgment that these documents do not contain all the features contained in the '525 Patent claims because the inventors' management had not approved them, and because the inventors continued to work on the design.

Based on the record, I must conclude that Cirrus failed to establish the alleged earlier invention date. The burden of production rested on Cirrus to enter evidence of the earlier conception of the invention, and this burden could not be satisfied solely by the oral testimony of the inventors, per the rule articulated in Mahurkar. The corroborating documentary evidence offered by Cirrus fails, by its own admission, to illustrate the earlier conception of the '525 Patent because certain significant claimed features such as a video port cannot be found in the architectural proposals. CFF 238, 240, 244, 246, and 247. As such they were not enabling. See e.g. Spero v. Ringold, 377 F.2d 652, 660 (CCPA 1967) ("A priority of conception is established when the invention is made sufficiently plain to enable those skilled in the art to understand it"). Under the circumstances, then, as to the absent claimed features, Cirrus provides nothing but the uncorroborated testimony of the inventors that they had

conceived of these claim elements at that time. Accepting such bare testimony is precluded by the "bright line" rule referenced in Mahurkar. Id. at 1577.

Although I reject Cirrus' bid for an earlier invention date for the '525 Patent, I find no clear and convincing evidence that the Oak Spitfire was on sale prior to January 23, 1994. Mr. Nguyen's testimony fails to provide a date certain, and his reference to "early" 1994 cannot satisfy the standard governing ATI's defense. The predictions contained in the two articles as to the available date also cannot meet the requisite standard. Therefore, ATI cannot prevail on its claim that the Oak Spitfire was sold prior to the '525 Patent's critical date. For the foregoing reasons, there is no need here to reach the parties' contentions regarding the technical features of Oak/Brooktree, as I conclude that the Oak/Brooktree fails to qualify as prior art for purposes of invalidating any of the asserted claims of the '525 Patent under Section 102(b). The evidence does indicate, however, that the Oak Spitfire and the Bt885 were sold prior to the '525 Patent invention date of January 23, 1995, such that the Oak/Brooktree will be considered as prior art under Section 102(a), and separately addressed in the section of this initial determination concerning the Section 102(a) defense, *infra*.

2. Intel i750

ATI relies heavily on the deposition testimony of Dr. Lawrence Ryan, a co-architect of the Intel i750, as well as Intel documents to argue that both pre-critical date printed publications describing the Intel i750, and the device itself, sold before the critical date, constitute anticipatory prior art references that invalidate all of the asserted claims of the '525 Patent. As to the Intel i750, Cirrus does not dispute prior art status, but focuses instead on arguments that certain limitations of each of the asserted claims cannot be found in the Intel

i750, such that a finding of anticipation would be improper. The Staff asserts that the Intel i750 does not, by Dr. Peuto's own admission, retrieve video data during the active display period, and therefore does not meet the "as ... rastered" limitation of Claim 13. Thus, the Staff concludes that the Intel i750 does not anticipate Claims 13, 15, 16, 17 or 23. However, as to Claim 37, the Staff argues for anticipation, based on the opinion to that effect by Cirrus' own expert, Mr. Ferraro.

Although not directly raised by the parties, I find that the Intel i750 does not anticipate or render obvious any of the asserted claims of the '525 Patent because it fails to meet the "frame buffer" and "multi-format frame buffer" elements common to all these claims. ATI asserts in its brief and its proposed findings of fact that [

] See RFF 678-680. Apparently, then, the [

] Neither Cirrus nor the Staff disputes this factual assertion, despite the fact that Cirrus provides a response to one of the ATI proposed factual findings containing this assertion, where Cirrus makes an unrelated clarification. [21]

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[21] Cirrus' failure to raise an objection based on the "frame buffer"/"multi-format frame buffer" limitations is not puzzling, as the Intel i750 meets *Cirrus'* proposed construction of the terms, which I rejected in construing the claims, *supra*.

The Staff's position with respect to these claim limitations in the Intel i750, however, appears inconsistent with its position on claim construction. While the Staff asserts the invalidity of Claim 37 as anticipated by the Intel i750 based solely on a concession to that effect by Cirrus' expert, Mr. Ferraro, the Staff and Cirrus sharply disagree on the proposed construction of the term "multi-format frame buffer" found in Claim 37, and using the *Staff's proposed definition,* Intel i750 does not meet this claim element. Therefore, the Staff's position as to the anticipation of Claim 37 by the Intel i750 is inconsistent with its position on the proper construction of the "multi-format frame buffer" limitation of Claim 37, which required that both regions of memory be able to store both graphics and video data.

Based on the correct construction of "frame buffer" from Claims 13, 15, 16, 17 and 23, and "multi-format frame buffer" from Claim 37, as applied to the Intel i750, I must conclude that the product fails to satisfy these claim elements, and therefore fails to anticipate the asserted claims. The [

] precludes anticipation. Accordingly, the parties' disputes regarding the Intel i750's satisfaction of other claim terms need not be addressed. Because ATI offers no specific obviousness argument as to these absent claim limitations, I also reject its obviousness defense based on the Intel i750, in connection with other prior art.

3. Parallax 1280/Viper

ATI argues that the Parallax 1280/Viper, sold prior to the critical date, anticipated Claim 13 and Claim 37, and, in combination with other prior art references, renders Claims 15, 16, 17 and 23 obvious. In support of this invalidity claim, ATI relies on the live testimony of the architect of the Parallax 1280/Viper, William Mears, a demonstration of the product, and on various documents and articles concerning the Parallax 1280/Viper. ATI contends that because the 1280/Viper was on sale nearly a decade prior to the '525 Patent filing date, the Parallax 1280/Viper qualifies as "on sale" prior art such that the "inner workings" of this device need not have been disclosed to the public to bring it within Section 102(b), pursuant to J.A. LaPorte, Inc. v. Norfolk Dredging Co., 787 F.2d 1577, 1583 (Fed. Cir.), cert. denied, 479 U.S. 250 (1986). Cirrus and the Staff do not dispute the prior art status of the Parallax 1280/Viper.

Cirrus raises several arguments against anticipation of these claims by the Parallax 1280/Viper. Its first argument, again stemming from its now-rejected proposed interpretation

of "controller", must fail, as this term does not mandate single chip, integrated architecture, and the Parallax 1280/Viper otherwise satisfies this element. Second, Cirrus distinguishes the Parallax 1280/Viper from Claims 13 and 37 on the grounds that that product [

] ATI claims that

[[22]] but Cirrus

contends that the [ ]

Based on my construction of the first and second pipeline limitations of Claim 13, the [

]

However, ATI cites the [

] Cirrus

responds that ATI should not be permitted to rely on this GOV16 mode, on the grounds that it failed to offer comprehensive evidence about the features and functionality of the Parallax 1280/Viper in this mode, and instead offered evidence only on the separate pipeline issue. ATI disagrees, responding that the evidence established that the normal mode and GOV16 modes are identical except that the latter has additional memory and two buses.

I conclude that ATI failed to offer clear and convincing evidence regarding the functioning of the Parallax 1280/Viper in GOV16 mode. Mr. Mears' testimony served as essentially the primary or at least sole comprehensive source of information regarding the operation of this mode. His testimony, however, contains internal inconsistencies on significant aspects of the Parallax 1280/Viper in the GOV16 mode. In particular, at the

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[22] [

] Mears, Tr. at 936.

hearing, Mr. Mears initially unequivocally stated that [

]

Mears, Tr. at 935. Moments later, though, [

][23] [

] Mears, Tr. at 936. Such internal inconsistency and lack of clarity on critical issues precludes me from relying on Mr. Mears' testimony as clear and convincing evidence of the functionality of the Parallax 1280/Viper in GOV16 mode. For the foregoing reasons, I reject ATI's anticipation and obviousness defenses based on the Parallax 1280/Viper, as there is a lack of the requisite evidence for application to the claims at issue.

C. Section 102(a) - Known by Others

35 U.S.C. § 102(a) provides that no entitlement to a patent exists where:

> the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent....

In its Post-Hearing Brief, under the heading for this invalidity defense, ATI merely references the earlier section of its brief on anticipation. In that earlier section, ATI asserts in passing

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[23]Mr. Mears had previously stated that he would use "V" and "G" to refer to data streams, but that "V" and "G" did not refer to "video" and "graphics".. Mears, Tr. at 936.

that Oak/Brooktree and the Parallax 1280/Viper also serve as invalidating prior art for purposes of Section 102(a), as these products practiced certain of the asserted claims and pre-date the invention of the '525 Patent. In its Reply Brief, ATI relies only on Oak/Brooktree "and certain associated documents" under Section 102(a), and no longer cites the Parallax 1280/Viper under this invalidity ground. For their positions in response to this invalidity defense, the other parties also merely incorporate by reference their discussion on anticipation by these same products.

ATI argues that Oak/Brooktree embodied Claims 13, 15 and 37, such that the invention of these claims of the '525 Patent was publicly known or used by others in this country prior to the '525 Patent's January 23, 1995 invention date, through both the product and the written descriptions described above. As set forth above, of the Oak/Brooktree prior art cited by ATI, I found the two articles and the slides not to be enabling, and I found that no clear and convincing evidence showed that the technical documents were made freely and publicly available more than one year prior to the '525 Patent application date. Under this subsection of Section 102, however, the prior art need only qualify as earlier than the invention of the '525 Patent, deemed to be January 23, 1995. The record reflects that a final Oak Spitfire specification dated September 1994 was shared with the public prior to January 23, 1995, and further that the Oak Spitfire and the Bt885 were sold to the public prior to January 23, 1995. Accordingly, it becomes necessary to compare Oak/Brooktree to Claims 13, 15 and 37 from a technical standpoint. ATI also makes an obviousness defense for the invalidity of Claims 16, 17 and 23 in view of Oak/Brooktree in combination with other prior art.

Although not raised by the parties, I conclude that clear and convincing evidence does

not establish that Oak/Brooktree satisfies the "frame buffer" or "multi-format" frame buffer elements present in all of the asserted claims of the '525 Patent. The technical documents, as well as the testimony of Mr. Siann [ ] indicate that in the Oak/Brooktree, the on-screen area of the frame buffer memory stored only graphics data, and not video. See RX 254; Siann Tr. at 1009-10, 1068; [ ] Accordingly, given the absence of this pervasive claim element, the Oak/Brooktree does not invalidate any claims of the '525 Patent under Section 102(a), and, because ATI offers no obviousness argument as to this missing element, the Oak/Brooktree does not render any of the claims of the '525 Patent obvious under Section 103.

To the extent ATI maintains its argument for this defense based on the Parallax 1280/Viper, my ruling, *supra*, with respect to ATI's failure to provide clear and convincing evidence of the functionality of the 1280/Viper in GOV16 mode, results in a rejection of this defense as to this prior art.

D. Section 102(e) - Patented by Others

35 U.S.C. § 102(e) provides that no entitlement to a patent exists where:

> the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent....

ATI asserts the invalidity under Section 102(e) of Claim 37 in light of U.S. Patent 5,406,306 ("Siann '306 Patent") and the Bindlish '864 Patent, and of Claim 13 in light of U.S. Patent 5,608,864 ("Bindlish '864 Patent"). ATI further argues the obviousness of the remaining

asserted claims based on these same two patents. As with anticipation, this defense will be considered separately from the indefiniteness findings, to the extent possible.

1. The Siann '306 Patent

The Siann '306 Patent issued on April 11, 1995, and was based on an application filed prior to the '525 Patent invention date. According to ATI, the Brooktree Bt885, discussed previously in connection with anticipation, was an embodiment of the Siann '306 Patent, such that ATI's arguments with respect to the Bt885 apply equally to the Siann '306 Patent. ATI notes as distinctions, however, that the Siann '306 Patent teaches a backend video pipeline and a backend graphics pipeline, as well as an output selector controlled by window logic and color key detector circuits. ATI admits that this patent does not disclose the "first port", "circuitry for writing", "second port", and "circuitry for generating an address" limitations of Claim 13, or the interpolation using dual FIFOs limitations of Claims 16, 17 and 23. ATI argues, however, that these elements were well known in the art so as to render obvious their combination with the Siann '306 Patent invention.

Cirrus first contends that because the Siann '306 Patent was before the patent examiner for the '525 Patent, ATI cannot overcome its more difficult burden to establish invalidity based on this reference, and second asserts that ATI failed to offer at the hearing the requisite evidence on the Siann '306 Patent, although the patent itself is in evidence. Both Cirrus and the Staff also assert that the Siann '306 Patent does not disclose the "circuitry for selectively retrieving" limitation included, explicitly or by dependence, in all the '525 Patent claims at issue. In support of this contention, Cirrus asserts that ATI's own expert conceded that this circuitry could not be found in the Siann '306 Patent.

Although ATI cites to certain "means for reading" graphics and video data[24] disclosed in the Siann '306 Patent as meeting the limitation, I find this insufficient to meet ATI's burden of clear and convincing evidence, particularly in the face of contrary assertions by both Cirrus' and ATI's technical experts. Cirrus correctly notes that the language cited constitutes "means plus function" language, limiting the means to those explicitly disclosed in the specification, and their structural equivalents. ATI's Dr. Peuto confirmed, at Tr. 1373-79, a previously given opinion on this claim element in the Siann '306 Patent, whereby he noted that these "means" were required by the claims but not disclosed in the specification. Such a situation is obviously problematic with "means plus function" language which necessitates disclosure in the specification. Based on my review of the Siann '306 Patent, ATI's failure to cite to anything in the specification of the Siann '306 Patent identifying the "means for reading" as "circuitry for selectively retrieving", and ATI's own expert's adverse opinion on this issue, I conclude that ATI has failed to meet its burden of showing by clear and convincing evidence that the Siann '306 Patent's reference to a first means for reading graphics and a second means for reading video discloses the "circuitry for selectively retrieving" limitation found in or applicable to all the asserted claims of the '525 Patent. In light of this ruling, Cirrus' additional arguments against finding that the Siann '306 Patent anticipated the asserted claims need not be individually addressed. Because ATI offers no obviousness argument with respect to this absent claim limitation, its obviousness argument also fails.

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[24]Claim 1 of the Siann '306 Patent sets forth "first means for reading the stored graphics pixels at a first frequency" and "second means for reading and storing the stored video pixels at a second frequency different from to [sic] the first frequency." Siann '306 Patent, Column 9, lines 55-59.

2. The Bindlish '864 Patent

ATI asserts the invalidity of Claims 13 and 37 of the '525 Patent as anticipated by the Bindlish '864 Patent, and further asserts the invalidity of Claims 15, 16, 17 and 23 as obvious in view of the Bindlish '864 Patent in combination with other prior art. The Bindlish '864 Patent issued on March 4, 1997 as a result of an application filed on April 29, 1994. As a threshold matter, the parties dispute the prior art status of this patent, with ATI claiming it was filed before the proven January 1995 invention date of the '525 Patent (the date of its issuance), and Cirrus and the Staff contending that the fall 1993 conception date of the '525 Patent invention precludes the Bindlish '864 Patent from qualifying as prior art. Having rejected, *supra*, Cirrus' claim to the earlier conception date, accordingly, the Bindlish '864 Patent must be considered prior art to the '525 Patent.

Turning to the technical aspects of the Bindlish '864 Patent, Cirrus' own expert conceded that if that patent were deemed prior art, it would invalidate Claim 37, and Cirrus explicitly adopts that admission. Cirrus Post-Hearing Brief at 93, Fn. 18. As to Claim 13, Cirrus asserts that the "always rastering" limitation is not satisfied, and Cirrus makes the further argument that no video port is found in the Bindlish '864 Patent.

As to the video port, ATI notes that the Bindlish '864 Patent teaches a "second port for receiving real-time video data" and "circuitry for generating an address associated with a selected one of said memory spaces for a word of said real-time video data." Cirrus contends, however, that ATI's expert, Dr. Peuto, admitted that the Bindlish '864 Patent does not disclose a video port into memory as required by Claim 13. ATI responds that Cirrus has mischaracterized Dr. Peuto's testimony, although ATI fails to explain the nature of the

mischaracterization. ATI also asserts that Cirrus' own expert implicitly acknowledged in his expert report that the Bindlish '864 Patent includes a live video port and circuitry for generating addresses. ATI urges examination of the patent itself for indications of the live video port and circuitry.

Although in his expert report, Dr. Peuto opined that the Bindlish '864 Patent included a video port and circuitry for generating an address, at the hearing, he retracted this opinion. When confronted on cross examination with the Bindlish '864 Patent references he relied on for his opinion, he admitted that these references failed to disclose a memory address generation circuitry for a video port. Peuto, Tr. at 1517. In its post-hearing submissions, when ATI attempts to rejuvenate the video port and address generation circuitry by relying directly on the Bindlish '864 Patent, ATI cites to exactly the same references that Dr. Peuto examined at the hearing to conclude that the address generation circuitry for the video port was not clearly set forth. In light of ATI's repeated insistence that Cirrus be bound by the admissions of its expert, it seems appropriate that ATI should be bound by Dr. Peuto's admission, particularly where he explicitly addressed the references on which ATI seeks to rely to contradict Dr. Peuto's opinion.

Turning, finally, to the "always rastering" limitation, Cirrus contends that ATI has failed to meet its burden of showing that the Bindlish '864 Patent meets this claim limitation. Cirrus notes that the Bindlish '864 Patent states that the CRT address counter stops during the Motion Video Window (MVW) display, such that the retrieval of graphics would also stop. Furthermore, Cirrus cites testimony by ATI's expert, Dr. Peuto, that the CRT Serializer circuitry is inactive during that same time, and Cirrus argues that because this is part of the

control circuit for the graphics pipeline, the pipeline must be inactive during the MVW display. In support of its position, ATI maintains first that the claim limitation only requires that data be rastered "to" not "through" the graphics pipeline, so that if data is always sent to the CRT Serializer, even if it stops there, this satisfies the limitation. Second, ATI relies on a statement in the Bindlish '864 Patent specification that "the data pipeline is kept full" coupled with testimony by [ ] Third and finally, ATI cites other testimony by [

]

I conclude that ATI has not met its burden of establishing the presence of this claim limitation by clear and convincing evidence. As to ATI's third argument, as I indicated in connection with the Nordic product, I find the testimony by [ ] on this issue not at all clear and therefore will not rely on it for the proposition advocated by ATI. I do not find ATI's argument distinguishing between "to" and "through" persuasive, as it flies in the face of the meaning of this limitation conveyed by the '525 Patent when reviewed in its entirety. Turning then, to ATI's assertion regarding the graphics backend pipeline being "kept full", this does not constitute clear and convincing evidence that data is always being rastered to the graphics pipeline, particularly where the specification indicates that the CRT Serializer, to which data from the CRT FIFO is transferred and from which data is output, may be stopped, and Dr. Peuto testified that the CRT Serializer is in fact not active during the MVW display period, Tr. at 1515. [25] Under these circumstances, it seems possible to interpret these factors

[25] ATI also maintains that its position is supported by the fact that the claim language states, that the CRT address counter *may* be stopped, not that it *is* stopped. As noted above, however, ATI's own expert Dr Peuto testified that the CRT Serializer is in fact not active during

to indicate that no graphics data is being rastered to the graphics pipeline, but the pipeline, because the CRT Serializer is not active, remains full in its static state. Given this uncertainty, and the inconclusive nature of the testimony and evidence offered by ATI, I find that ATI has not satisfied its burden on this issue.

Accordingly, based on my review of the Bindlish '864 Patent and the opinion of Dr. Peuto, I conclude that ATI has failed to meet its burden of providing clear and convincing evidence that the Bindlish '864 Patent meets all limitations of Claim 13. Rather, the evidence suggests that it lacks the "circuitry for generating an address" and "always rastering" limitations of Claim 13, and as no obviousness arguments were offered, I conclude that the Bindlish '864 Patent even considered in combination with other prior art, does not invalidate Claims 13, 15, 16, 17 and 23 of the '525 Patent. However, given Cirrus' admission and the prior art status of the Bindlish '864 Patent, this prior art invalidates Claim 37 under Section 102(e).

E. Section 102(g) – Invented by Others

35 U.S.C. § 102(g) provides that no entitlement to a patent exists where:

> before the applicant's invention thereof the invention was made in this country by another who had not abandoned, suppressed, or concealed it. In determining priority of invention there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

ATI asserts the applicability of Section 102(g) based on Brooktree's Bt885, discussed

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the MVW display period, and I note that ATI has argued with respect to certain positions advanced by Cirrus, that a party should not be heard to argue a contrary position from that of its expert.

supra, because it allegedly embodied the asserted claims of the '525 Patent, was conceived by late 1992 and diligently reduced to practice. As set forth above, in connection with ATI's Section 102(a) defense based on Oak/Brooktree, the Bt885 did not practice the asserted claims of the '525 Patent, and so does not invalidate them under Section 102(g).

F. Section 102(f) - Derivation of Invention

Although ATI originally raised this invalidity defense, and included it in the Joint Narrative Statement of Issues ("JNSI"), in its post-hearing brief, ATI expressly withdraws this defense. ATI Post-Hearing Brief at 102.

G. Section 103

Section 103 sets forth the requirement that the subject matter of a patent be non-obvious. The patent should not be obtained if:

> ...the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

35 U.S.C. § 103(a) (1998).

An obviousness determination involves an analysis of the prior art from the perspective of one of ordinary skill in that art at the time of the patent in question, including consideration of whether there existed an explicit or implicit suggestion to combine particular pieces or features of the prior art. Graham v. John Deere Co., 383 U.S. 1, 17 (1966); Env. Instruments, Inc. v. Sutron Corp., 877 F.2d 1561, 1568 (Fed. Cir.), cert. denied, 119 S.Ct. 56 (1998). The obviousness challenger must show some teaching or suggestion in the prior art to make any combination or substitution of features on which the challenger relies. Fromson v. Anitec Printing Plates, Inc., 132 F.3d 1437, 1447 (Fed. Cir. 1998). To make the determination

regarding such a teaching or suggestion, the following factors may be considered for a motivation to combine or substitute: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. In re Rouffet, 149 F.3d 1350, 1355-56 (Fed. Cir. 1998).

ATI makes numerous obviousness arguments in conjunction with its discussion of other invalidity grounds that rely on the same prior art. As threshold assertions, ATI contends that at the filing date of the '525 Patent, the art of combining computer graphics and video was "old and crowded", and that the level of ordinary skill in the art was quite high. Next, ATI highlights certain claimed features absent from many of the prior art references it relies on, and argues the obviousness of combining these claimed features, vertical interpolation, color keying, real-time video capture, and address-generating circuitry with the cited prior art.

ATI raises its obviousness defense as to some or all of the '525 Patent claims based on the Nordic product, Oak/Brooktree, the Intel i750, the Parallax 1280/Viper, the Siann '306 Patent, the Bindlish '864 Patent and the Cirrus Pixel CL-PX2070/CL-PX2080 or its upgrade, the 2085("2070/2080"). As to all the prior art except the 2070/2080, the obviousness issue has already been considered and decided. In making those obviousness rulings as well as this one, I have considered the scope and content of the prior art and the expert testimony regarding the level of skill in the field at the time of the '525 Patent. I have also taken account of secondary considerations, such as the customer demand and priorities for video graphics display controllers, which indicate that the type of architectural innovations claimed by the '525 Patent were not readily obvious to one of ordinary skill in the art because, given the age of some of the cited prior art, and the customer demand, they would likely have been implemented sooner.

decoding, where does the address decoding take place in the '525 patent?

"Answer: In the CPU interface 206."

Was anything I read inconsistent with our front-end processing construction of claim 13?

A No.

Q Later, because I didn't believe you, I have to admit, I kept pressing. Later we came back to this, and I asked you whether you were sure that this did not relate to back end processing. At page 206, beginning at line 20, "question: Well, you said that the CPU interprets data as either graphics or video-based on its aperture address?

"Answer: Yes.

"Question: And then the data is placed in the frame buffer; correct?

"Answer: Correct.

"And then that data is retrieved from the frame buffer; correct?

"Answer: Correct.

"Question: And the data is forwarded to either the video or graphics pipeline; correct?

"Answer: I think we're getting beyond the scope of this.

"Question: Well --

"Answer: I'm not sure how that ties into answering the question.

"Question: Well, if you could just bear with me a little while, maybe we'll get through it. Do you remember the last question? The data retrieved from the memory buffer is directed into either the video or graphics pipelines; correct?

"Answer: That wasn't your last question. I thought your question was from the CPU interface, how the data is directed into either video or graphics, and you're talking about front-end processing. You've switched over to back-end processing.

"Question: Oh, I see. So you're interpreting the first port limitation here as a strictly front-end operation?

"Answer: Yes.

"Question: So the processing as a word of video data or a word of graphics data, you would describe to be so-called front end pipelines of the '525 patent?

"Answer: Yes."

Again, Mr. Schafer, you were educating me that this first port limitation is only, only directed to front-end processing; isn't that true?

A That appears to be the case.

Q And you made a point of making sure I understood that there was a mechanism within the first port for decoding the address associated with a particular word of data and directing it into either the front-end video or front end graphics pipelines; correct?

A Correct.

Q And you differentiated this mechanism from the dual aperture port saying that it could be something that forwards data to either the front-end video or graphics pipeline but did not have to be the dual aperture port; isn't that right?

A That's right.

Q And your interpretation of the first port limitation of claim 13 is that it includes any mechanism for taking an address associated with a data word and using that address to direct the data into either the front-end video pipeline or the front end graphics pipeline; correct?

A As we've just discussed, yes.

Schafer, Tr. at 660-64.

111. Mr. Ferraro testified that the "first port" limitation refers to the host port or PCI port, through which the CPU sends video and graphics data accompanied by addresses. Ferraro, Tr. at 489.

112. The term "frontend" is used to describe an element of a video graphics display controller which sits between the frame buffer and the host processor. Nally, Tr. at 134.

113. The term "backend" is used to describe an element of a video graphics display controller which sits between the frame buffer and the monitor. Nally, Tr. at 134; Ferraro, Tr. at 494.

114. Cirrus' Pre-Hearing Brief stated that the "first port" limitation of Claim 13 " . requires a

first

port through which data is received with addresses that tell the claimed device whether the data is video or graphics so that it will be properly processed." Cirrus Pre-Hearing Brief at 25.

115 In diagrams he prepared in connection with his review of the '525 Patent, Mr. Ferraro represented the "first port" by noting "video or graphics?" next to an "address" identification. RX 504C at CL 120271; Ferraro, Tr. at 816-17.

116. The '525 Patent shows a VPORT interface 211 for receiving real-time video data. CX 1, Fig. 2.

117. The '525 Patent specification states: "Real-time video source 104 may be, for example, a CD ROM unit, a laser disk unit, a videotape unit, television cable outlet or other video data source outputting video data in a YUV format." CX 1, Column 5, lines 13-16.

118. Video is typically in YUV format. Ferraro, Tr. at 491.

119. Dr. Peuto stated that "video is now a term that is generally used to mean photorealistic real-time images encoded in YUV like television." ALJ 1 at 101.

120. The '525 Patent specification states: "Circuitry 201, 202 is provided for generating an address associated with a selected one of the memory spaces for each word of received real-time video data." CX 1, Column 3, lines 16-19.

121. The '525 Patent specification states: "In this instance, VGA controller 105 generates the required addresses into frame buffer 107." CX 1, Column 5, lines 11-13.

122. The '525 Patent specification states: "Data which is input through the video port 211 [is] address-free. In this case, video window controls 213 generates the required addresses to either the on-screen memory area or the off-screen memory as a function of display

location for the video window." CX 1, Column 5, line 66 - Column 6, line 3

123. Data received through the second port does not come in with addresses and, therefore, it is necessary to generate addresses for the incoming data so that it can be placed in the frame buffer. Ferraro, Tr. at 491.

124 The '525 Patent specification states: "Circuitry is also provided for selectively retrieving the words of data from the on-screen and off-screen spaces as data is rastered for driving a display." CX 1, Column 3, lines 21-23.

125. Mr. Ferraro testified, without offering support for this opinion, that "circuitry for selectively retrieving" means that each word can be selectively retrieved so that you are not forced to retrieve word 3 after word 2, but you would have the option, for example, of retrieving word 1 followed by 100. Ferraro, Tr. at 492.

126. Mr. Schafer affirmed his deposition testimony that:

> 'Selectively retrieving refers to the retrieval of graphics data within a graphics region, and the retrieval of video data within a video region of the display, and it doesn't necessarily mean at any point in time because the -- obviously, you have to grab the data ahead of time to display it. So there is some prefetching involved there. The selection is based upon the existence of a video window or existence of a graphics display and its position.'

Schafer, Tr. at 666.

127. At the end of each scan line, the scanning beam returns to the start of the next line. The periods of time during which the beam returns to the next line are called the "retrace" periods. ALJ 1 at 12-13.

128. Mr. Ferraro also described the definition of "rastered" as follows:

Now, rastered, the viewable area on the screen is called the raster. The area of the screen in which data is displayed is called the raster People refer to rastering the display as the providing of data to the display. Rastering also has a connotation of a two-dimensional, one-dimensional to a two-dimensional transformation so that we have a wire providing data to the monitor. That's one-dimensional, and that data is then parsed onto the screen in a two-dimensional fashion. You might use the term a typewriter rasters type onto a page, left to right, top to down format. "As data is rastered for driving a display" is a very important limitation in my mind.

Ferraro, Tr. at 492

129. Mr. Ferraro opined that:

> Rastering is the retrieval, processing, and providing of data from a frame buffer memory to a CRT/LCD display for the purpose of displaying pixel data .... The screen is refreshed by scanning a beam across the two-dimensional surface in a left-to-right and top-to-bottom sequence across the screen .... This process of providing data in a two-dimensional fashion is called rastering. In its most common usage, rastering implies the production of two-dimensional data to a CRT as retrieved from frame buffer memory.

CX 745C at 9 (Ferraro Expert Report).

130. Regarding the definition of "rastered" in the "circuitry for selectively retrieving" limitation of Claim 13, Mr. Ferraro testified as follows:

> A I think that the rastering there is referring to the providing of data to the display.
> Q In your expert report, you write -- and this is at page 9 of the report, which is under tab 3, "rastering is the retrieval processing and providing of data from the frame buffer memory to a CRT LCD display for the purpose of displaying pixel data." Is that consistent with your definition here in claim 13?
> A Yes. As I said when we first started the questioning regarding rastering, that I felt that it was a -- it was used as a metaphor, that it meant different things in different places, but the process of retrieving

data to put it on the screen is, in the largest sense, in my mind, rastering than the actual providing of the data onto the screen, that's also using the term rastering. And rastering out of memory is the more directed towards the memory, retrieving data out of memory. So I think it can be all three of those. I think it's used in all three.

Q So rastering is more than any one discrete element, it is a process; correct?

A No, that's not what I meant to say. What I meant to say is, in the one usage of the term, it's a process from start to finish. In another usage of the term, it relates to the retrieving of data out of memory. And in another usage of the term, it relates to putting data onto the screen, but it's -- the term "rastering" is used because it's that two-dimensional to one-dimensional transformation, or one-dimensional to two-dimensional.

Q The question is in the context of as data is rastered for driving a display, is rastered there a process or a discreet operation?

A I think there it's a bit of both. I don't think either conflict. I think you could read that to say as data is rastered for driving a display. Since you're already retrieving that data, that would indicate, okay, you're retrieving the data for the process of rastering to the display, and then it could also be read more tightly to say you're selectively retrieving the data as the data is being rastered onto the display. So I think that you could interpret it -- I think that you could interpret rastered in either of those contexts.

Q So it could mean both the discreet -- well, so it means, in your opinion, in this context, it means both a discreet [sic] operation of sending the data to the display as well as the process for getting it there?

A Yeah, I think it could be either one.

Ferraro, Tr. at 1654-55.

131. Mr. Ferraro explained the display raster as follows:

So what we saw is the dot going across the screen in sort of a typewriter fashion, one dot being displayed at a time, and this is referred to as "refreshing" a line. So a line of data is refreshed. Now, after the line of data is refreshed, just like our antique typewriters, it has to get back to the previous line. We do a carriage

return feed so it zips and comes back, ready to type the next line or display the next dot. This is called retracing or blanking, because no data is actually displayed in this time. It's just meant to get this scanning device back to the start of the next line ready for the next peice [sic] of data ... Afterwards, we have a retrace period where the beam is going down to the next line. This entire period of time represents the refreshing of one line, including the time to get back and ready for the next line.

ALJ 1 at 12.

132. Dr. Peuto refers to the active raster scan as the "active display period." Peuto, Tr. 1380

133. Mr. Ferraro also testified that in some contexts, "rastering" refers to a process of providing data to the display including the processing of data in the pipeline. Ferraro, Tr. at 1651.

134. Mr. Nally testified that "rastering" is taking data from the memory and sending it to the display device. Nally, Tr. at 174-75.

135. Mr. Nally's testimony supports an understanding of "raster" to include the entire process of retrieving and displaying data, with the entire display process, not just the active raster scan included. Nally, Tr. at 174-75.

136. The '525 Patent specification states:

In the preferred embodiment, data is continuously pipelined from on-screen memory through graphics back-end pipeline 205 to the inputs of output multiplexer 231. Window data from off-screen memory however is only retrieved from memory and pipelined through video backend pipeline 204 when a window is being displayed. In other words, when a window has been reached, as determined by control bits set by CPU 101 in VW control registers 222, video window display controls 222 generate addresses to retrieve the corresponding data from the off-screen memory space of frame buffer 107. Preferably, video FIFOs 223 and 224 are filled before the raster scan actually reaches the display window such that the initial pixel data is available immediately once the window has been reached. In order to insure that graphics memory data continues to be provided to graphics back-end pipeline 205, video window display controls 222 "steal" page cycles between page accesses to the graphics memory. It should be noted that

once the window has been reached the frequency of cycles used to retrieve window data increases over the number used to fill the video FIFOs when outside a window. When the frequency of window page accesses increases, video window display controls 222/arbiter 221 preferably "steal" cycles from page cycles being used to write data into the frame buffer.

CX 1, Column 9, lines 43-57.

137. A "pipeline" refers to a sequence of processing stages where the output of one becomes the input of another, and so on, in "assembly line" fashion. CX 745C at 12 (Ferraro Report); ALJ 1 at 83-84.

138. The '525 Patent specification states: "A first pipeline 205 is provided for processing data received from the on-screen area of frame buffer 107." CX 1, Abstract, lines 11-13.

139. The '525 Patent specification states: "A graphics backend pipeline processes ones of the graphics words of data retrieved from the frame buffer." CX 1, Column 3, lines 24-25.

140. Figure 2 of the '525 Patent shows the elements of backend graphics pipeline 205. None of the circuitry of the backend graphics pipeline is shared with the video pipeline 204. CX 1, Figure 2.

141. The "first pipeline" disclosed by Claim 37 processes for display graphics data retrieved from the frame buffer, and is therefore a backend pipeline. See CX 1, Column 19, lines

142. Mr. Ferraro testified that the video and graphics backend pipelines represent distinct and separate paths for the video and graphics data. Ferraro, Tr. at 500.

143 The '525 Patent specification states: "A second pipeline 204 is provided for processing data retrieved from the off-screen area of the frame buffer " CX 1, Abstract, lines 13-15.

144. In the first IDS to the Patent Office in connection with the '525 Patent application, prior art was distinguished from the '525 Patent invention based on the prior art not disclosing

"a pair of output pipelines for separately processing graphics (RGB) and video (YUV) data retrieved from the single frame buffer." CX 2 at 144.

145. The figures in the '525 Patent do not indicate that the graphics backend pipeline shares circuitry or elements with the video backend pipeline. CX 1

146. The '525 Patent never makes reference to or suggests shared circuitry or elements between the graphics backend pipeline and the video backend pipeline. CX 1.

147. No party offered evidence that one skilled in the art would understand that two distinctly identified pipelines with different functions could share circuitry or elements.

148. The '525 Patent specification states: "... CRT controller 220, through arbiter 218 and memory interface 219, maintains a constant stream of graphics data into graphics backend pipeline 205 from memory; video or playback graphics data is rastered out only when a window has been reached by the display raster as determined by display position controls of window controls 222 (see FIGS. 3 and 5 and accompanying text) and CRT controller 220." CX 1, Column 8, lines 23-29.

149. The '525 Patent specification states: "... the static graphics are rastered out of the on-screen memory without interruption and passed through the graphics backend pipeline 205. The window of data in off-screen memory is rastered out only when the display position for the window has been reached by the display raster and is passed through video backend pipeline 204." CX 1, Column 6, lines 55-61.

150. Mr. Ferraro testified that this "always rastering" claim element means "that it's necessary to always retrieve the graphics data, so that even in those pixels that you're going to display video data, you still need to retrieve graphics data." Ferraro, Tr. at 495

151. The '525 Patent specification states: "In order to insure that graphics memory data continues to be provided to graphics back-end pipeline 205, video window display controls 222 'steal' page cycles between page accesses to the graphics memory. It should be noted that once the window has been reached the frequency of cycles used to retrieve window data increases over the number used to fill the video FIFOs when outside a window. When the frequency of window page accesses increases, video window display controls 222/arbiter 221 preferably 'steal' cycles from page cycle being used to write data into the frame buffer." CX 1, Column 9, lines 57-67.

152. The '525 Patent specification states: "A video backend pipeline is provided for processing ones of the video words of data retrieved from the frame buffer, the circuitry for retrieving always rastering a stream of graphics data from the frame buffer to the graphics pipeline and rastering video data to the video backend pipeline when a display raster scan reaches a display position of a video window." CX 1, Column 3, lines 25-32.

153. The '525 Patent specification states: "Memory control circuitry 201 includes an arbiter 218 and a memory interface 219. Arbiter 218 prioritizes requests for access to frame buffer 107 received from video front-end pipeline 200, graphics controller 208 and bit block transfer circuitry 209. Arbiter 218 further sequences each of these requests with the refresh of the display screen of display 106 under the control of CRT controller 202 " CX 1, Column 8, lines 7-14.

154. Mr. Bicevskis gave the following testimony:

> Q Now, there's actually an arbiter in the memory controller of the Rage Pro that prioritizes requests; correct?

A That's correct.

Q And the arbiter needs to do that because the memory controller gets requests for data or requests for -- access to memory, to be more precise, get requests for access to memory from a variety of functional blocks in the Rage Pro; correct?

A That is correct.

Q So it will get a request for a retrieval from, say, the graphics pipeline, and that might compete with a request for a retrieval from a video pipeline; correct?

A That is correct.

Q And indeed, it might compete with a request for a writing of data to memory from the memory controller; correct, not from the memory controller. Where does that request for writing come from?

A That would come from the host port.

Q So it has to --

A If it's host data coming in or it could come from a 2D entry or 3D entry.

Q So there are a variety of requesters for access to memory in the Rage Pro?

A That is correct.

Q So sometimes some of those requesters have to wait while the arbiter decides to give priority to another requester; is that correct?

A That's correct.

Q And that results in delays in the retrieval of data, delays as perceived, if you will, by the requester?

A That is correct.

Q And this is true for the Rage LT Pro and the Rage 128; correct?

A As well as any controller that uses DRAM.

Q Because this is a generic memory controller; right?

A Also by the nature of DRAM, you have to do things like refresh cycles, which means that you will, by definition of the device, stall the retrieval times.

Q So it's essentially inherent in the current design of display controllers that there will be -- that there needs to be the functionality of allocating access to memory in some sort of prioritized fashion among the various requesters?

A That is an accurate statement.

Q And indeed, it is virtually inherent in the design of a modern display controller that is perceived by any one of those requesters, there may well be delays in the access to memory that it has requested?

A That is correct.

Bicevskis, Tr at 299-301.

155. The '525 Patent specification states: "Preferably, video FIFOs 223 and 224 are filled before the raster scan actually reaches the display window such that the initial pixel data is available immediately once the window has been reached." This refers to "prefetching". CX 1, Column 9, lines 54-57.

156. When "rastering" is used in connection with a memory retrieval operation, it includes prefetching. See CX 1, Column 6, lines 25-26 ("... both graphics and video data may be rastered *from the frame buffer* ...").

157. According to Mr. Ferraro, in the '525 Patent, video data only has to be retrieved when it is required to refresh the video portion of the window. Ferraro, Tr. at 537.

158. According to Mr. Ferraro, it makes no engineering sense to interpret "when" to mean "at the exact instant." A number of circuit elements sit between the monitor and the frame buffer. "All circuitry elements are going to impose a delay." Ferraro, Tr. at 538.

159. Delays inherent in rastering video data to the video backend pipeline include clocking delays, gate delays, arbiter imposed delays on the access to the frame buffer, and processing delays in the video backend pipeline. Ferraro, Tr. at 538-40.

160. It would be impossible for an engineer to "design a system that had no delay such that data can be retrieved instantly at the moment the CRT is at a particular point. . . There is no engineer that would be able to do that. It's not physically possible." Ferraro, Tr. at

545.

161. Mr Ferraro stated that he does not "understand the meaning of when in this claim to be the exact same instant. When, in the context of this particular circuitry, means at the same time, given the necessary throughput delays of the related circuitry." Ferraro, Tr. at 552.

162. Mr. Ferraro identified Column 9, lines 54 through 60 of the '525 Patent as supporting an interpretation of "when" that allows for timing delays. CX 745 C at 62 (Ferraro Rebuttal Report).

163. Mr. Ferraro's preferred interpretation of "when" is that it means "in response to," in other words as data is needed for the video window. Ferraro, Tr. at 1647.

164 Mr. Schafer testified that "[o]bviously you have to grab the [video] data ahead of time to display it. So there is some pre-fetching involved there." Schafer, Tr. at 666. Mr. Schafer further testified that video "data must be fetched ahead of time or it could not keep up with the display. So the actual existence of [a] video window does have a bearing on when data is fetched, but it's not fetched at the precise moment that a pixel is to be output for display on the monitor." Schafer, Tr. at 667.

165. Mr. Bicevskis testified as follows:

> Q Now, Mr. Bicevskis, it would be quite hard to design a system that retrieved from memory -- let me set it up a little bit more clearly. We've got an arbiter. It's dealing with requests from various circuitry elements. We're back in January 1995. Then we've got FIFOs and we've got -- in the video pipeline.
>
> So we have the video pipeline stages that you and I discussed in your first testimony. And the arbiter as we discussed is a little unpredictable sometimes in figuring

out -- in determining when the video information is going to be displayed.

So with that set of assumptions, Mr. Bicevskis, isn't it true that it would have been very difficult -- I'm not going to say impossible, because who knows what's impossible. I'll be more of an engineer with you, very difficult to design a system in which circuitry for retrieving video data, sent it to the video pipeline at the same time a raster scan reached a video window display position on the screen?

A That's correct.

Bicevskis, Tr. at 1255-56.

166. Mr. Bicevskis agreed that it would be very difficult to design circuitry that could retrieve video data, send it to the video pipeline at the same time a raster scan reached a video window position on the screen. Bicevskis, Tr. at 1256.

167. Mr. Bicevskis agreed that several circuit elements related to the retrieval of data from memory impose delays on the data retrieval. Bicevskis, Tr. at 299-301.

168. Mr. Bicevskis' "hallway analogy" testimony regarding the feasibility of a system where video data is retrieved at the exact instant that the display raster scan reaches the display position of a window necessarily requires that "rastering" in the context of the "when" limitation not include pre-fetching. Bicevskis, Tr. at 1265-67.

169. "Rastering" in the context of the "when" limitation includes pre-fetching. See CX 1, Column 15, line 52 ("... rastering a stream of data *from said frame buffer* ..." (emphasis added)).

170. Mr. Ferraro testified as follows:

Q Let me ask it this way. Yesterday, you described the "when" condition as allowing for a certain amount of delay between the occurrence of the condition and the

retrieval of data from the frame buffer; isn't that true?

A Yes.

Q And so under your rubric, under your analysis, the condition you specified was, at a time prior to the display raster scan reaching the display window, the result being that you take data out of the frame buffer and pass it through the video pipeline; correct?

A Given the delays in the system, that was one of two possible meanings that I agree with.

Q I just want to make sure that the result is not in dispute. It doesn't sound like it's in dispute. The thing that has to happen is we're taking data out of the frame buffer and passing it through the video pipeline; correct?

A The rastering of data to said video back-end pipeline has to occur, and that is correct. I don't like saying that it is a result because I don't want my words turned against me -- meaning that I agree to your condition, but not the result. Okay.

Q Sure. We're going to talk about the condition. Let's go ahead and do that. So now there are two possibilities for the condition that I think I heard you say yesterday. Now, there are two possibilities. The first is that this when condition means "at the time that." So when would be replaced with at the time that a display raster scan reaches a display position of a video window.

A Are you including delays in that?

Q No, I'm not.

A But that's not consistent with the specification language.

Q Perhaps, and again, you and I are going to talk a lot about that. I'm just trying to get down on the board the two possibilities that I believe you identified yesterday. One was that this happens at the time that the display raster scan reaches the video window, and the other was at a certain time prior to the time that the display raster scan reaches a video window.

A Because is the time -- are you saying at the exact instant of time?

Q Yes, this means at the exact instant. Condition 1 -- or interpretation 1 means at the exact instance.

A Can you write exact on there, please.

Q At the exact time. And 2 was the other possibility that you offered, which was, I believe, at a

time prior to the exact time

A That would be fine, yes.

Q The exact time, so those are two possibilities?

A I would like you to please qualify "prior" in that it's not just any arbitrary time prior It's time prior with respect to engineering practice and as specified in the '525 specification.

Q Okay. Well, let's talk about that. How long prior?

A That's design-specific.

Q You can't tell us how long prior; isn't that right?

A If I was to look at any particular design and then knowing as we all agree that the arbiter introduces unpredictable delays, also given the fact that we have a two-dimensional system and not a one-dimensional system so that you can't -- you can say okay, I want to delay a certain number of pixels to the left because we have pixels, but you can't say I would like to go three quarters of a line ahead. You have to go pixels and lines in increments of 1. So given that, given a design, an engineer of average skill in the art could determine what the delay would need to be as specified in the '525 specification.

Q Okay. Let's just use the patent. I'm looking at the video pipeline, which is element 204 in figure 2; isn't that right?

A Yes.

Q And FIFO A seems to be the first, and then we've got decoder 225, interpolator 226, interpolator 227, color space converter 228, and then pixel doubler 237. Is that the video pipeline shown here in figure 2 of the '525 patent?

A Is that the video pipeline that you believe to be there?

Q I'm asking you, is that it?

A Yes, that is what I believe to be there.

Q All right. So the question is, how long is the delay through this video pipeline?

A There's a lot of parameters that feed into that. I think that the one that -- as I said, there's implementation-specific things with, how many delay stages do you have in your DAC? As Mr. Bicevskis indicated, there's delay in your scaler. As I indicated, whether

you're zooming or diminuating determines how much there is in the scaler. The FIFO, depending on what's happening, the FIFO determines it and then most important -- not most important, but most unpredictably, the arbiter in the circuit retrieval search.

Ferraro, Tr. at 719-23.

171. Mr. Ferraro also testified as follows:

Q So as I count back from the left edge of the video window, I'm going backward in time; correct?
A Yes, sir.
Q Now, I'm going to start counting the pixels back, and I want you to tell me when it is that I am beyond the time prior to the exact time as you define the "when" in the condition we're discussing in claim 13.
A I think in order for me to do that, we're going to have to talk about specific implementation. Would you like me to interpret the '525 and, as an electrical engineer and designer, design a system and tell you how I would do it?
Q I want you to focus on the '525 patent, on the system disclosed in the '525 patent.
A I am, sir, focusing on the '525 patent and the '525 patent is an architectural patent. I can't answer that question any more than I can answer the question how many AND gates are there in the scaler. That's a detail which is implementation-specific.

Ferraro, Tr. at 725.

172. Dr. Peuto testified as follows:

Q Well, 10 [sic], what does when mean to you?
A At this point it is -- it is probably possible to design a product that will do this, but it's more interesting to read the specification itself to try to find some guidance about what is the meaning of the word "when."
Q And what did you find when you read the specification?
A I have an exhibit that I can use to illustrate that.
Q This now is Exhibit RDX-34; is that correct?

A Yes.

Q Please use that.

A This is an exhibit in which we have taken an element of the '525 drawings called figure 3, which I believe is in its entirety, and we have taken a part of what I believe is figure 3, which is a figure that describe the type of signals that are driving the multiplexer, and the type of signal that are driving the multiplexer in that figure, the multiplexer is multiplexer 231, and it has some input that are the graphics and some inputs that are the video pipeline.

And the port called A and B are what makes you that you select either A or B -- excuse me, either the video or the graphics to then go to the latch and the DAC. And the implication, as we said, is the monitor is after the DAC 210. So this drawing suggests that between the comparisons of the screen raster scan and the definition of the window extent of the video window, there is very few gate delays that takes place before this signal is provided first through this multiplexer 304 and then to the line B of multiplexer 231.

So the fact that we had very few gate delays would suggest that the interpretation for the word "when" would be when taking into account those claim delays. I want to explain what is the likely value of those claim delays. We are talking a few nanoseconds in the kind of technology we're talking about. A nanosecond is a billionth of a second. So it's a very small amount of time.

Very often in the discussion, we have used the word "pixel time." This is because it's also a simple unit to use. On a 1024 by 768 monitor refreshing 72 times per second, the time it takes to draw one pixel to the next is 12 nanosecond, 12-1/2 nanosecond. So when we talk few nanosecond, we are in essence talking about few pixel time worth of time.

So then I conclude when I take this figure and the text that goes with it that explain things in more details, when I take this constraint from the specification and import it into the meaning of the claim, I find that I should expect to really start doing the fetching few pixel times before, which is what I mean to indicate by drawing a red rectangular region, which is offset in time, time, you know, move from left to right, offset in time by few pixel,

and although I probably have two or three in my drawing.

Q Dr. Peuto, based on your reading of the '525 patent, when does the circuitry in that patent start to retrieve data from the memory that's going to be displayed on the screen?

A Few pixel times before it hits the window.

Q And how does that relate to the diagram that you have there in front of you to your right?

A It is the time that it takes from those comparison to be prop you will gated to the --

Q And how -- what's your understanding of how Cirrus interprets the when portion of this claim?

A My understanding is Mr. Ferraro has come with a position that would say few pixel times before, like the same position I'm taking.

Peuto, Tr. at 1350-53.

173. The instantaneous retrieval of video data for display upon the active raster scan reaching the video window constitutes an engineering impossibility. Schafer, Tr. at 666-67; Ferraro, Tr. at 538, 545; see also Bicevskis, Tr. at 1255-56, 1260-62.

174. Persons of ordinary skill in the art would understand that the retrieval of video data for display involves some inherent engineering delays, and may involve pre-fetching, such that some of the retrieval is done in advance of the display. Peuto, Tr. at 1351-53; Ferraro, Tr. at 538, 545, 552; Schafer, Tr. at 666-67.

175. Cirrus did not present testimony or evidence regarding the understanding of one of ordinary skill in the art as to the amount of time in advance that pre-fetching should or would occur, or the amount of time that should or would be taken in video retrieval by engineering delays.

176. Cirrus' expert, Mr. Ferraro, testified that the length of time for pre-fetching or other engineering delays associated with video retrieval could not be quantified based on the

'525 Patent, but was design-specific. Ferraro, Tr. at 725.

177. Cirrus argues that the "when" limitation must "tak[e] into account predictable *and unpredictable* delays in retrieving and processing data." Cirrus Post-Hearing Brief at 43 (emphasis added).

178. The '525 Patent specification states: "An output selector is included for selecting for output between words of data output from the graphics backend pipeline and words of data output from the video backend pipeline." CX 1, Column 3, lines 32-35.

179. The '525 Patent specification states: "[T]he inputs to output multiplexer 231 are ... 16 or 24-bit color data directly from graphics backend pipeline 205 serializer 236 and 24-bit color data from the color look-up table 234 ...Depending on the mode, color comparison circuitry 302 compares selected bits from the overlay color key register 303 with either the 8 bits indexing look-up table 234 in the color look-up table mode (pseudocolor mode) or the 16-bits (24-bits in the alternate embodiment) passed directly from serializer 236." CX 1, Column 10, lines 4-28.

2. Claim 15

180. Claim 15 of the '525 patent reads as follows:

15. The controller of claim 13 wherein said output selector is operable to:

in a first mode, pass only a word of data output from said graphics pipeline;

in a second mode, pass a word of data output from said video pipeline when said display raster scan has reached a display position corresponding to a window and a word of data from said graphics pipeline when said display raster scan is in any other display position;

in a third mode, pass a word of data output from said video pipeline when said display raster scan has reached a display position corresponding to a window and a corresponding word of data from said graphics pipeline matches a color key and a word of data from

said graphics pipeline when said display raster scan is in any other display position; and

in a fourth mode, pass a word of data from said video pipeline when said corresponding word of data from said graphics pipeline matches a color key and a word of data from said graphics pipeline when said display raster scan is in any other display position.

CX 1.

181. Claim 15 depends on Claim 13. CX 1.

182. No dispute exists among the parties as to the proper construction of the "first mode" limitation of Claim 15

183. The '525 Patent specification contains a description of the output selector circuitry. CX 1, Column 10, lines 1-14; Column 11, line 61 - Column 12, line 35. Claim 15 itself contains no such description of the output selector circuitry. CX 1.

184. According to Mr. Ferraro, the first mode means that the whole screen is being filled only with graphics data, and that only graphics data is passed. Ferraro, Tr. 557, 1602.

185. The '525 specification states: "In a second mode, a window of data is rastered from the off-screen memory when the display raster scan has reached the display window position and graphics data being rastered from the on-screen memory matches a color key." CX 1, Column 2, lines 55-59.

186. The "when" condition in the "second mode" limitation of Claim 15 refers to a different event than that referred to in the "when" limitation of Claim 13. With respect to the event referred to in Claim 15, the specification does not cite or describe any necessary delays or any pre-fetching of data. CX 1.

187. Mr. Ferraro testified as follows regarding Claim 15:

> ... In the second mode, pass a word of data output from said video

pipeline when said display raster scan has reached a display position corresponding to a window.

I want to break the claim element at that point. Our "when" word has popped up again. Now, here we're talking about when, but this time we're talking about -- if we're looking at it as a temporal relationship, we're not talking about a when which is going to pass data from the output of the video pipeline to the monitor.

Now, if we're talking temporally how much delay, there we can easily see it's going to be less delay than all the way back to the memory. So when, this use of the word "when" is consistent with both of my definitions, because it applies both to in response to, that the output selector has to passes the video data when the display, raster is at the video window in response to, and also when with the necessary delays.

Now, even at this far back end part of our device, still you can't read it instantaneously because there are still delays between the output selector and the final, just a lot less delay and perhaps more predictable delay than the full path of the data. And we continue 13B, and a word of data from said graphics pipeline when said display raster scan is in any other display position, so we've already described that case where we have a video window somewhere on the screen and all around it is the graphics data. The graphics data is going to be provided all around it, and the video data is going to be provided inside of it. So this mode precludes any graphics data from being displayed inside the video window. It's always video window inside, always graphics data outside.

Ferraro, Tr. at 557-58.

188. In practice, the "when" condition in the "second mode" limitation of Claim 15 does not by necessity involve the same degree of engineering delays or pre-fetching as are involved in the case of retrieving data in Claim 13, and in Claim 15's second mode, these delays are more predictable in nature. Ferraro, Tr. at 557-58. ATI offered no expert testimony to contradict Mr. Ferraro on this point.

189. According to Mr. Ferraro, the "second mode" limitation teaches the passing of video data in the video window, ignoring color keying. Ferraro, Tr. at 1603.

190. The '525 Patent specification states: "In a third mode, the window data is rastered out of the off-screen memory when the data being output from the on-screen memory matches the color key, notwithstanding the position of the raster scan." CX 1, Column 2, lines 59-62.

191. Mr. Ferraro testified that the "third mode" limitation allows for graphics data to be displayed inside the video window. This allows graphics data to occlude video data in the video window. Ferraro, Tr. at 560.

192. Mr. Ferraro testified that the "third mode" limitation teaches that both color keying and the window position have to be satisfied for the passage of data. Ferraro, Tr. at 1604.

193. Mr. Ferraro explained that color keying requires the selection of a particular color for use as the key. If the graphics data matches that color, then video is selected for display. ALJ 1 at 31-32.

194. Dr. Peuto explained color keying as "selecting two streams of data and you're making a choice based on a specific key, a specific color, a choice that was predetermined before . . ." ALJ 1 at 87-88.

195. The '525 specification states: "[T]he inputs to output multiplexer 231 are ... 16 or 24-bit color data directly from graphics backend pipeline 205 serializer 236 and 24-bit color data from the color look-up table 234 ...Depending on the mode, color comparison circuitry 302 compares selected bits from the overlay color key register 303 with either the 8 bits indexing look-up table 234 in the color look-up table mode (pseudocolor mode)

or the 16-bits (24-bits in the alternate embodiment) passed directly from serializer 236."

CX 1, Column 10, lines 4-28.

196. Dr. Peuto asserted "And a word is a collection of byte[s]." ALJ 1 at 102.

197. In the third mode of Claim 15, the data from the graphics pipeline that is compared against the color key value consists of a "word". CX 1, Column 16, lines 6-12, Column 10, lines 4-28.

198. According to Cirrus and Mr. Ferraro, the "fourth mode" limitation teaches that window position is to have no effect on the decision to pass video. Ferraro, Tr. at 1605.

199. Mr. Schafer testified as follows:

> Q Now we get to the fourth mode.
> A Within the video.
> Q Within the video window; correct?
> A That's right.
> Q Now we get to the fourth mode, and the fourth mode is kind of a mixed metaphor, isn't it?
> MR. JACOBS: Your Honor, I'm going to have to object on -- I know you had cautioned us, but a mixed metaphor question I just don't understand.
> JUDGE MORRISS: Could you rephrase it, please.
> BY MR. CORDELL:
> Q Well, Mr. Schafer, the fourth mode of claim 15 is unclear to you; isn't that right?
> A It's confusing.
> Q In fact, it is missing an essential statement about what to do when inside the video window; isn't that right?
> A It says "in any other display position" without stating the display position. So it's confusing.
>
> Schafer, Tr. at 623-24.

200. Dr. Peuto testified as follows:

> Q And then the fourth mode?

A I have to tell you I can't parse that fourth mode.
Q What's the word you were using?
A I cannot parse it. I cannot understand it.
Q What's the difficulty you have with it?
A It's the issue of certainly saying "is in any other display position," and at this point I just do not know what this claim is meant, and your Honor, as you may know -- I just don't.

Peuto, Tr. at 1357.

201. Cirrus changed its position as to the proper construction of the "fourth mode" limitation between its post-hearing brief and its reply brief. Cirrus Post-Hearing Brief at 57; Cirrus Reply Brief at 30.

202. The reference to "when said display raster scan is in any other display position" in the "fourth mode" limitation is inconsistent with an exclusively color key system. In the context of a description of a color key system, the reference to "when said display raster scan is in any other display position" is nonsensical and unintelligible. See Peuto, Tr. at 1357; Schafer, Tr. at 623-24.

203. "[A]ny *other* display position", as set forth in the "fourth mode" limitation, lacks an antecedent reference. CX 1; Schafer, Tr. at 623-24..

3. Claim 16

204. Claim 16 of the '525 Patent reads as follows:

16. The controller of claim 13 wherein said video pipeline includes a first first-in-first-out memory for receiving a plurality of words of data for a first display line of pixels in memory and a second first-in-first-out memory or receiving a plurality of words of data from a second display line of pixels in memory.

CX 1.

205. Claim 16 depends on Claim 13. CX 1.

206. The '525 Patent specification does not define the meaning of a "first-in-first-out memory." CX 1

207. The term FIFO is well known to a person of ordinary skill in the industry as a memory structure in which data are written into the memory in the same order they are read out of the memory, hence the name first-in-first-out. Peuto, Tr. at 1360, RX-617C at 12, CX 745C at 13 (Ferraro Expert Report).

208. Neither of the FIFOs taught by Claim 16 operates as a write buffer, holding data destined for memory, as such a finding would be inconsistent with the description of the function of the FIFOs in the '525 Patent specification as receiving data for the generation of the on-screen display. CX 1, Column 8, lines 33-36, lines 44-51.

209. "Display line" is the pixel data that represents the information to be put on the monitor. Ferraro, Tr. at 688.

210. The phrase "display line of pixels in memory" refers to the pixel data that represents a horizontal display row on the monitor. Ferraro, Tr. at 688; see also ATI Post-Hearing Brief at 50.

4. Claim 17

211. Claim 17 of the '525 Patent reads as follows:

> 17. The controller of claim 16 wherein said first display line is stored adjacent in memory to said second display line.

CX 1.

212. Claim 17 depends on Claim 16. CX 1.

213. "Adjacent" means that in two-dimensional space adjacent lines are one directly above the

other. In one-dimensional space, the lines are horizontally neighboring. Ferraro, Tr. at 689.

214. Mr. Schafer testified as follows:

> Q Claim 17 says that the first display line that stored adjacent in memory to the second display line. Can you give us your understanding of that phrase?
>
> A That the pixels in the first display line are stored sequentially from some address, and immediately after the last pixel in the first display line, the pixels from the second display line are stored sequentially from that address on.
>
> Q Now, turning back in the specification to column 8, line 40, it refers to a pair of lines as being N minus 1 and N plus 1 in memory. Do you see that?
>
> A Yes, I do.
>
> Q Does this mean that these two lines would, in fact, not be adjacent in memory?
>
> A I would say that this is talking about source lines N minus 1 and N plus 1 which would indicate to me there's a two line separation in memory, not adjacent.

Schafer, Tr. at 630.

215. Mr. Ferraro testified as follows:

> Q And with respect to -- can you comment on claim 17, please?
>
> A Claim 17 requests that the said first display line is stored adjacent in memory to said second display line. Now, in memory, we have this storage in the left to right contiguous memory of our lines of data. And this claim is stating that the first display line is stored adjacent in memory to the second display line, and in the specification, it describes adjacent display lines, and it also has in my opinion a typographical error, and it talks about two display lines being N minus 1 and N plus 1, and I have to confess it took me twice to realize that that is a mistake, that N minus 1 and N plus 1 are not adjacent and that really N minus 1 and N would be adjacent or N and N plus 1 would be adjacent. I think the use of the word adjacent is pretty

well known and that that can be written off as a typographical error.

Ferraro, Tr. at 687.

216. ATI points to no expert testimony by its technical experts regarding the meaning of the adjacent storage in Claim 17.

5. Claim 23

217. Claim 23 of the '525 Patent reads as follows:

23. The circuitry of claim 13 wherein said video pipeline comprises:

a first-in/first-out memory for receiving a first stream of words of data from said frame buffer;

second first-in/first-out memory disposed in parallel with said first first-in/first-out memory for receiving a second stream of words of data from said frame buffer; and

interpolation circuitry for selectively generating an additional word of data by interpolating a word of said first stream and a word of second stream data output from said first and second first-in/first-out memories.

CX 1.

218. Claim 23 depends on Claim 13. CX 1.

219. The '525 Patent specification states: "Backend video pipeline 204 further includes a Y interpolator 226 and X interpolator 227." CX 1, Column 8, lines 62-63.

220. The '525 Patent specification states: "An interpolator is provided as part of the video pipeline for generating additional data by interpolating data output from the first and second first-in/first-out memories." CX 1, Column 3, lines 64-67.

221. The '525 Patent specification states: "The output of X interpolator 227 is passed to a color converter 228 which converts the YCrCb data into RGB data for delivery to output

multiplexer 304." CX 1, Column 9, lines 8-10.

222. The '525 Patent specification states: "In the preferred embodiment, during Y zooming (expansion) Y interpolator 226 accepts two vertically adjacent 16-bit RGB or YCrCb pixels from the decoder 225 and calculates one or more resampled output pixels using a four subpixel granularity. X interpolator 227 during X zooming (expansion) accepts horizontally adjacent pixels from the Y interpolator 226 and calculates one or more resampled output pixels using a four subpixel granularity. For data expansion using line replication, Y interpolator 226 is bypassed. Y interpolator 226 and X interpolator 227 allow for the resizing of a video display window being generated from one to four times " CX 1, Column 8, line 62 - Column 9, line 7.

223. Interpolation differs from replication: in replication you simply copy each pixel, in interpolation you estimate new values of what should be in between two existing pixels. ALJ 1 at 36-37.

224. Dr. Peuto explained the difference between replication and interpolation: "The simplistic mechanism . . . deals with replicating the pixels and the more complex mechanism does some averaging operation on the pixels in order to be able to blow up the image and have less granularity." ALJ 1 at 92-93.

B. <u>Whether ATI's Rage Devices Infringe the Inserted Claims</u>

1. Claims 13 and 37

225. The ATI Rage Devices are video and graphics controllers. Bicevskis, Tr. at 266; Peuto, Tr at 1339.

226. The ATI Rage Devices have a frame buffer divided into on-screen and off-screen

memory areas. Bicevskis, Tr. at 1112-13, 1120.

227. The ATI Rage Devices store [

] CFF 498; Bicevskis, Tr. at 1120.

228 The ATI Rage Devices [

] Bicevskis, Tr. at 1120; Peuto, Tr. at 1534.

229. Mr. Ferraro testified that the ATI Rage Devices have circuitry for writing selectively words of received data into the on-screen or off-screen memory. Ferraro, Tr. at 508-09.

230. The ATI Rage devices have circuitry to selectively write graphics and video data into on-screen or off-screen memory according to the addresses accompanying the data. Bicevskis, Tr. at 277-78, 284-85.

231. The ATI Rage Devices have a bus interface [

] ATI Post-Hearing Brief at 30-31; RFF 271; Bicevskis, Tr. at 277-78, 284-86.

232. Mr. Bicevskis explained [

] Bicevskis, Tr. at 279, 283.

233. Dr. Peuto believes the ATI Rage Devices meet the "second port" limitation of Claim 13. Peuto, Tr. at 1345

234. Mr. Ferraro testified that the ATI Rage Devices have a video port for receiving real-time video data. Ferraro, Tr. at 518-19.

235. The ATI Rage Devices have a video port for receiving real-time video data. Peuto, Tr. at 1345; Ferraro, Tr. at 518-19

236. Mr. Bicevskis testified as follows:

[

]

Bicevskis, Tr. at 295-96.

237. Mr. Ferraro testified that [

] Ferraro, Tr. at 521.

238. The ATI Rage Devices contain circuitry for generating an address associated with a selected one of the memory areas for real-time video data received through the video port. Bicevskis, Tr. at 295-96; Ferraro, Tr. at 521.

239. Mr. Bicevskis testified as follows:

[

]

Bicevskis, Tr. at 296-99

240. Mr. Bicevskis testified [

] Bicevskis, Tr. at 301-02.

241. Mr. Bicevskis' testimony from transcript pages 296-302 indicates his inclusion of both graphics and video data in his description of the retrieval of "data". Bicevskis, Tr. at 296-302.

242. Mr. Bicevskis testified [

] Bicevskis, Tr. at 1200.

243. The ATI Rage Devices contain circuitry for selectively retrieving graphics and video data from on-screen and off-screen areas as data is rastered for driving a display. See Bicevskis, Tr. at 296-302; 1000-001.

244. The ATI Rage Devices have a graphics backend pipeline and a backend video pipeline. Bicevskis, Tr. at 303-04.

245. In testifying to the existence of the graphics backend pipeline and the video backend pipeline, Mr. Bicevskis never stated or suggested that they shared circuitry or elements. Bicevskis, Tr. at 303-04.

246. Dr. Peuto testified as follows:

[

]

Peuto, Tr. at 1341-42, 1347.

247. ATI offered no affirmative evidence that the ATI Rage Devices' graphics backend pipeline and video backend pipeline share circuitry or elements.

248. The graphics backend pipeline and the video backend pipeline in the ATI Rage Devices [ ] See Bicevskis, Tr. at 303-04; Peuto, Tr. at 1341-42, 1347.

249. The ATI Rage Devices' retrieval from the frame buffer and sending of data to the graphics backend pipeline [ ] Bicevskis, Tr at 304, 307.

250. The ATI Rage Devices contain circuitry for retrieving always rastering a stream of data from the frame buffer to the graphics backend pipeline. See Bicevskis, Tr. at 304, 307.

251. The ATI Rage Devices retrieve video data [

] Peuto, Tr. at 1546-1547

252. In light of its indefiniteness, the "when" limitation of Claim 13 cannot be applied to the ATI Rage Devices for purposes of an infringement analysis.

253. The ATI Rage Devices have output selector circuitry to select between data output from the graphics backend pipeline and data output from the video backend pipeline. Peuto, Tr at 1354; Ferraro, Tr. at 556.

2. Claim 15

254. In light of its indefiniteness, Claim 15 cannot be applied to the ATI Rage Devices for purposes of an infringement analysis.

3. Claims 16, 17 and 23

255. The ATI Rage Devices contain [ ] See Hall, JX 8C at 89; Bicevskis, Tr. at 317, 324, 1147; Schafer, Tr. at 600-01, 624-26; Nally, Tr. at 157.

256. The ATI Rage Devices do not contain two FIFOs. Peuto, Tr. at 1358-60; Bicevskis, Tr. at 327-28, 1174.

257. A line buffer serves as a delay element that accepts and holds data. Ferraro, Tr. at 685-86.

258. In the ATI Rage Devices, [ ] Ferraro, Tr. at 685-86.

259. The line buffer(s) in the ATI Rage Devices perform the same function and achieve the same result as the dual FIFOs described in the '525 Patent. Ferraro, Tr. at 679-87.

260. Oswin Hall [

] Hall, JX 8C at 89-99.

261. Oswin Hall [

]

Hall, JX 8C at 91-92.

262. Mr. Ferraro offered credible expert testimony that, from the standpoint of one skilled in the art, the ATI Rage Devices' line buffer(s) constitutes an equivalent both to the first FIFO and to the second FIFO set forth in the '525 Patent. Ferraro, Tr. at 672-89.

263. Mr. Ferraro's testimony [

] Ferraro, Tr. at 672-89; Hall, JX 8C at 89-99.

264. Dr. Peuto testified as follows:

[

]

Peuto, Tr. at 1359-60 (emphasis added).

265. Dr. Peuto's testimony at Tr. 1359-60 regarding the ATI Rage Devices' line buffers is inconsistent with Mr. Hall's statements regarding the functionality of the ATI Rage Devices' line buffer(s). Peuto, Tr. at 1359-60; Hall, JX 8C at 89-99.

266. The ATI Rage Devices' line buffer(s) is equivalent to the dual FIFOs described in Claims 16, 17 and 23 of the '525 Patent.

III. Validity

A. On-Sale Bar

267. It is conclusively established for purposes of this investigation that Cirrus offered for sale CL-GD7542 Nordic product ("Nordic Product") in the United States before January 23, 1994. See Cirrus Notification (4/27/99).

268. Cirrus offered no direct evidence that the Nordic Product was *not* placed on sale in the U.S. before January 23, 1994.

269. Cirrus' Robert Dickinson testified as follows:

[

]

Dickinson, Tr. at 391.

270. Mr. Dickinson never directly testified that Cirrus made no offer to sell the Nordic Product prior to January 23, 1994. See Dickinson, Tr. at 336-429.

271. Cirrus identified [

]

272. In 1993, Cirrus [

]

273. [

]

274. [

]

275. [

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276. [

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277. [

]

278. [

]

279. [

]

280. No party offered direct evidence of actual sales of the Nordic Product prior to January 23, 1994.

281. [

]

282. [

]

283. [

]

284. [

]

285 The Nordic Product invention was ready for patenting as of January 23, 1994. See *supra*.

286. [

] [ ]

287. [

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288. [

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289. [

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290. [

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291. [

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292. [

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293. [

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295. [

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297. [

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298. [ ]

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301. [

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302. [

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303. [

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304. [ ]

305. [

306. [

]

307 [ ]

308. As to Claim 37, Cirrus raises no technical arguments against the Nordic Product practicing this claim. Cirrus Post-Hearing Brief; Cirrus Reply Brief.

309. As to Claim 13, Cirrus limits its arguments against the Nordic Product practicing this claim to the video port/address generation circuitry and the "always rastering" limitations Cirrus Post-Hearing Brief; Cirrus Notification (4/27/99).

310. The indefiniteness of the "when" limitation of Claim 13 precludes application of that claim limitation to the Nordic Product.

311. [

]

312. [ ]

313. [

]

314. [

]

315. [

]

[

]

[

]

316. In the passage quoted above, [ ] seemed to misunderstand the questioning, to lack the necessary knowledge to respond, or to provide nonresponsive answers. [

]

317. The Nordic technical specification does not clearly and directly indicate whether the Nordic Product satisfied the "always rastering" limitation, and neither party offered adequate expert testimony to clarify the specification. See CX 102C.

318. When confronted on cross examination with certain statements from the Nordic 1M Specification and the Nordic Preliminary Data Book, Dr. Peuto was not able to explain why he concluded that the Nordic 7542 continued to retrieve graphics even when it was displaying video data. Peuto, Tr. at 1501-10.

319. Dr. Peuto testified that the CRT address counter relates to fetching graphics data into the graphics FIFO. Peuto, Tr. at 1502. Dr. Peuto further admitted that when video is displayed, the CRT address counter is stopped to avoid a wrong count, meaning that the retrieval of graphics data from memory and into the "incoming port" of the graphics FIFO is stopped. Peuto, Tr. at 1502-04. Dr. Peuto asserted that graphics data would continue to flow out of the graphics FIFO into the rest of the graphics pipeline, and that the graphics FIFO would need to be refilled once it was emptied. However, Dr. Peuto did not point to any specific evidence in the Nordic documentation to support this point, nor did he assert that graphics data would continue to be retrieved for each pixel location on

the screen. Peuto, Tr. at 1504.

320. ATI did not point to evidence as to the obviousness of combining the "always rastering" feature with the Nordic Product.

B. Section 102(b) – Anticipation

1. Oak/Brooktree

321. Oak/Brooktree refers to the combination of two products made by two different companies: the Oak Spitfire OTI-64107, and the Brooktree Bt885. Peuto, Tr. at 1364-68, see RX 239 (Brooktree Bt885 specification), RX 254 (Oak Spitfire specification).

322. Jonathan Siann was the architect for the Bt885 Siann, Tr at 990-92

323. Mr. Siann worked with Oak Technology to design the Oak Spitfire following the proposed architecture he designed for an interface with the Bt885. Siann, Tr. at 998.

324 The Oak Spitfire was designed to interface with the Bt885. Siann, Tr. at 1040; CX 745C at 58 (Ferraro Rebuttal Report).

325. The January 1994 Oak Spitfire specification contains a technical diagram showing both the Oak Spitfire product and the Bt885. See RX 254 at ATI 018065-66; Peuto, Tr. at 1364-68.

326. The Oak Spitfire and the Bt885 are separate chips. Peuto, Tr. at 1365.

327. The Bt885 was sold by the end of 1993. Siann, Tr. at 999.

328. The Oak Spitfire was sold prior to January 23, 1995. [

] Nguyen, JX 15C at 24.

329. An article published in the June 1993 edition of Electronic Design magazine referenced and discussed the Oak Spitfire product and the Bt885. Siann, Tr. at 999; RX 251C.

330. The Electronic Design article included a diagram similar to the drawing in Oak's Data Book (RX 250). Nguyen, JX 15C at 12.

331 ATI failed to point to any expert testimony from the perspective of one skilled in the art that the material in the June 1993 edition of Electronic Design includes an enabling description of the relevant architecture.

332. An article published in the July 5, 1993 edition of Electronic Engineering Times referenced and discussed the Oak Spitfire product and the Bt885. RX 252.

333. ATI failed to point to any expert testimony from the perspective of one skilled in the art that the material in the July 5, 1993 edition of Electronic Engineering Times includes an enabling description of the relevant architecture.

334. Mr. Siann gave a public slide presentation on the Bt885, with no nondisclosure agreement, at a conference in March 1993. Siann, Tr. at 994-95.

335. ATI failed to point to any expert testimony from the perspective of one skilled in the art that the material in Mr. Siann's slide presentation included an enabling description of the relevant architecture.

336. Mr. Nguyen, the Oak Spitfire project manager, testified that he could not recall whether [

]

Nguyen, JX 15C at 20-21, 23.

337. Mr. Nguyen testified that typically, engineering versions of specifications [

] Nguyen, JX 15C at 21.

338. ATI pointed no testimony other than Mr. Nguyen's regarding the public availability of the January 1994 Oak Spitfire specification [RX 254].

339. Mr. Nguyen testified that [

] Nguyen, JX 15C at 21.

340. Mr. Nguyen testified that he did not know [

] Nguyen, JX 15C at 21.

341. Regarding the invention date for the '525 Patent invention, Mr. Nally testified as follows:

> Q Let's see if we can get the chronology down. Do you recall when you were doing this thinking about a solution to the problem?
>
> A Yeah. It was over the summer of 1993.
>
> Q And what do you recall about the events of that summer in connection with this analysis? Do you recall some back-and-forth with management on your proposed solution?
>
> A Okay. I actually made -- during the summer, I was putting together my ideas. Either sometime late summer or early fall, I presented management with my first proposal, and they reviewed the proposal, and they actually rejected it. They said it was too risky. They thought it was overdone. And the reason why it was rejected is because I was at that point saying that we really need two video windows, not just one, but two video overlay windows.
>
> And the reason I was doing that, if you remember, I was working on the 2070 and 2080 and I still saw a great need for video conferencing. I was trying to bring not only multimedia to the PC but also teleconferencing capability to the PC. In order to bring teleconferencing to the PC, you needed two video overlay windows.
>
> So my proposal actually went further than what they asked for. They said give me just rudimentary video for windows playback mode, and I gave them something that was more than what they wanted. So they rejected it.

Q What happened next?

A I went back and redid my proposal. I toned it down. I reduced it down to one video window, left the video port in there, and resubmitted it.

Nally, Tr. at 66-67.

He subsequently testified that the second proposal was also rejected, and he continued his back-and forth with management. Nally, Tr. at 67-70.

342. Mr. Schafer testified as follows:

Q Mr. Schafer, I ask you to turn to tab 1 of your binder, which is a copy of the '525 patent, and I'd like to ask you, when did you begin working on the concepts that led to this patent?

A I began working on this in the summer of 1993 with Robert Nally and continued working on it through the fall of1993 and then into 1994.

Schafer, Tr. at 565-66.

343. Regarding work on the '525 Patent invention, Mr. Schafer testified as follows:

Q Let's turn to tab 2, which is CX-30. Can you tell us what this document represents?

A Yes. This was a architectural proposal generated by Robert Nally in the fall of 1993. It describes the state of our discussions at that time regarding this architecture.

Q Does this document reflect all the features that were finally implemented by you?

A No. It was the primary ideas, but we actually refined some of the sections over the course of the next couple of months, added more detail.

Q Let's turn to tab 3, which is CX-31, and can you tell us what the purpose of this document was?

A This is a later version of the document we just talked about distributed to more of the marketing and management team to indicate the current state of our progress on the architecture and to give a list of features and the current state and some detail on those features.

Q. Does this document reflect all of the details that you implemented?

A No. There were some pieces missing. Some of it is regarding the level of detail that we later developed, and some features were actually not included in the documentation that Robert was generating, primarily because they weren't approved -- in the approved features set from our management at the time. Robert and I had discussions on the insertion video port for capturing video. We had some of our own ideas we wanted implemented, but they weren't deemed important enough to delay the schedule for this product, so they were left out of the initial documentation.

Q Now, do you recall at the time that this document was generated whether you were actually working on those details that were left out?

A Yes. We had discussed the -- for instance, the video, we discussed that over the course of the summer because that was a feature we had in some of our existing products, not the video integrated, but stand-alone video. So the work was being done on this but not in this widely distributed documentation.

Q Was this the first proposal that Mr. Nally gave to management?

A I don't recall if this was the first or not. This was obviously not the first revision of this document, but I don't know if this is the first one that management saw.

Schafer, Tr. at 567-68.

344. The October 1993 and the November 1993 proposal documents by Mr. Nally, CX 30C and CX 31C, do not reflect the final structure of the '525 Patent invention; some features of the '525 Patent invention were not included on the documents. See CFF 238, 240, 244, 246, 247; Schafer, Tr. at 567-68.

345. See additional findings of fact regarding Oak/Brooktree, *infra*, under Section 102(a).

2. Intel i750

346 Dr. Lawrence Ryan was a co-architect of the Intel i750. Ryan, JX 23C at 16.

347. The Intel i750, manufactured by Intel Corporation, includes the 82750 Display Processor, the 82750 Pixel Processor and video digitizer circuitry. Peuto, Tr. at 1430-31, RX 492 at ATI 057155; RX 264 at ATI 019398.

348. The Intel i750 was on sale more than one year prior to the filing of the '525 Patent application, *i.e.* before January 23, 1994. Ryan, JX 23C at 13-18; RX 275C; RX 137; RX 276C.

349. The Intel i750 was in public use more than one year prior to the filing of the '525 patent application, i.e. before January 23, 1994. Ryan, JX 23C at 13-18; RX 275C; RX 137; RX 276C.

350. Both graphics and video data are stored in the frame buffer memory of the Intel i750 Ryan, JX 23C at 49, 75, Peuto, Tr. at 1324; Peuto Expert Report at 39 (RX 616C); Ferraro, Tr. at 1576-77.

351. The i750 frame buffer [

] Ryan, JX 23C at 50, 72-73; DB Guide at ATI019717, ATI019766 (RX 262C); RX 493C; RDX-23C.

352. The i750 memory has on-screen and off-screen areas. Ryan, JX 23C at 74-75; Peuto, Tr. at 1438-39; RX 493C; RDX-23C; Ferraro, Tr. at 1577.

353. In the i750, [

] Peuto, Tr. at 1438; RX 493C; RDX-23C.

354. In the i750, [

] Peuto, Tr. at 1438-1439; Ferraro, Tr. 1577; RX 493C; RDX-23C.

355. In the i750, [

] Peuto, Tr. at 1439; Ferraro, Tr. at 1577; RX 493C; RDX-23C.

3. Parallax 1280/Viper

356. Parallax Graphics Inc. sold the Parallax 1280 product beginning in early 1984, and sold the VIPER product beginning in 1988 (both products collectively referred to as "Parallax 1280/Viper"). Order No. 38 at 8.

357. The Parallax 1280 and the VIPER products have essentially the same features and functionality. RX 615 at 13.

358. Mr. William Mears was the architect of the Parallax 1280/Viper. Mears, Tr. at 863.

359. The Parallax 1280/Viper could operate in two modes: [

] Mears, Tr. at 892, 932-33.

360. In the normal, [

] Mears, Tr. at 892.

361. Mr. Mears' testimony served as the primary, or at least essentially the sole comprehensive source of information on the [ ]

362. Mr. Mears testified as follows:

[

]

Mears, Tr. at 935-37.

363. Mr. Mears' testimony contained internal inconsistencies and/or lacked clarity on certain aspects of the [ ] mode of the Parallax 1280/Viper, which were not clarified by other evidence. See e.g. Mears, Tr. at 935-37.

C. **Section 102(a) - Known by Others**

364. The Oak Spitfire and the Bt885 were sold to the public prior to January 23, 1995. Nguyen, Tr. at 16-17; Siann, Tr. at 999.

365. The Oak Spitfire specification dated [

] Nguyen, Tr. at 15-16.

366. The Oak Spitfire specification indicates that the frame buffer has "two different places", a "graphics data area" and a "video data area". RX 254 at ATI 018061.

367. Mr. Siann explained that in interfacing the Bt885 and the Oak Spitfire, the on-screen region of the frame buffer corresponds to graphics data, and the off-screen area corresponds to video data. Siann, Tr. at 1068.

368. In explaining his slide presentation on implementing the Bt885 with a product such as the Oak Spitfire, which had a single frame buffer, Mr. Siann stated that "...the biggest block in the frame buffer will be the on-screen graphics memory ...." Siann, Tr. at 1009-10

369 In explaining his slide presentation on implementing the Bt885 with a product such as the Oak Spitfire, which had a single frame buffer, Mr. Siann testified that the off-screen memory would typically store video but could also store other "things like fonts or cursors or more graphics." Siann, Tr. at 1012.

370. Mr. Siann's testimony indicates that when used in connection with the Bt885, video was only stored off-screen area of the Oak Spitfire frame buffer. See Siann, Tr. at 1009-10, 1068. Mr. Nguyen testified that [

] Nguyen, JX 15C at 40.

D. Section 102(e) – Patented by Others

1. The Siann '306 Patent

371. U.S. Patent No. 5,406,306 ("Siann '306 Patent") issued on April 11, 1995, and was based on an application filed on February 5, 1993. RX 4.

372. The Siann '306 Patent is related to the Brooktree Bt885. Peuto, Tr. at 1369; CFF 951

373. The '525 Patent applicants disclosed the Siann '306 Patent to the patent examiner during prosecution. CX 2 at 161-63.

374. ATI's expert, Dr. Peuto, was previously retained in connection with a lawsuit between Brooktree and S3 involving the Siann '306 patent. Dr. Peuto worked together with Dr. Ryan of Intel on that case. Peuto, Tr. at 1370-71.

375. In connection with the Brooktree/S3 litigation, Dr. Peuto worked together with Dr. Ryan on claim charts regarding the Siann '306 patent that were attached to a declaration that Dr. Ryan submitted in that litigation. In particular, Dr. Peuto worked on the "clarified function" and "structural notes" columns of those claim charts. Peuto, Tr. at 1371-76

376. In preparing his expert report on the '525 patent, Dr. Peuto relied on Dr. Ryan's declaration regarding the Siann '306 Patent and attached a copy of Dr. Ryan's declaration and accompanying claim charts to his expert report. Peuto, Tr. at 1371-72, RX 616C, Exhibit B.

377. The "clarified function" column of the expert report for the Siann '306 Patent repeatedly states with particular elements of the Siann '306 patent that "a display memory controller including fetch and address logic is required but not disclosed." RX 616C, Exhibit B at S301948, S301950, S301953, S301955, S301960, S301963, S301967, S301969, S301980. For example, this comment appears twice on S3-01980, with respect to two elements of claim 1 of the Siann '306 Patent: the "first means for reading the stored graphics pixels at a first frequency," and the "second means for reading and storing the stored video pixels at a second frequency . . ." Id.; see also RX 4, Column 9, lines 55-59 (Siann '306 Patent).

378. Dr. Peuto testified at his deposition in this investigation that he agreed with the comment in the "clarified function" column of the claim charts for the Siann '306 Patent that "a display memory controller including fetch and address logic is required but not disclosed." Peuto, Tr. at 1376-77.

379. Dr. Peuto confirmed at the hearing that he stood by the comment in the "clarified function" column of the claim charts for the Siann '306 Patent that "a display memory controller including fetch and address logic is required but not disclosed." Peuto, Tr at 1377-78. In particular, Dr. Peuto agreed that the specification of the Siann '306 Patent did not disclose a display memory controller including fetch and address logic. Peuto, Tr.

at 1378.

380. Dr. Peuto asserted that the claims of the Siann '306 Patent refer to a memory controller, but agreed that the patent did not disclose the specifics of such a memory controller. Peuto, Tr. at 1378-79.

381. Dr. Peuto testified as follows:

> Q Did you find the page I was referring to, Dr. Peuto?
> A You mean 1980?
> Q Yes.
> A Yes, I do.
> Q Okay. And I've put up here on the overhead CDX-146, which is a blow-up of this page. The way we've received it, it's rather difficult to read. Do you see that at the top that says "claim chart for U.S. patent number 5,406,306"?
> A Yes, I do.
> Q Okay. And then the left-hand column it says "claims"?
> A Yes.
> Q And actually, that's just the first -- okay. And then there's a column that says "clarified function." Do you see that?
> A Yes.
> Q Did you work with Dr. Ryan on the clarified function column?
> A I was one of the participant in that work.
> Q You were involved with it?
> A I was involved with it.
> Q Okay. And do you see that under "first means," the second paragraph under clarified function, it says at the end of the sentence "display memory controller including fetch and address logic is required but not disclosed." Do you see that?
> A Where is that?
> Q It's -- if you look at the screen, the overhead projection, that may help you find it. It's basically the second paragraph under --
> A First mean?

Q Yes.

A I see that.

Q Okay. And then under "second means," at the end of the sentence, the same sentence appears, do you see that?

A I see that.

Q Now, that means that when you were working with Dr. Ryan on this you concluded that the Siann '306 patent required fetch and address logic but did not disclose it; is that correct?

A That's what it says.

Q And it was correct when this was written; correct?

A I wouldn't say that.

Q Were you involved in writing this?

A No -- excuse me. I was involved in writing it.

Q Do you recall that Mr. Jacobs took your deposition and asked you some questions about that precise passage?

A I do.

Q I'd like to ask you to turn to your deposition, which is tab 1.

A Tab 1.

Q And at page 109, line 4, there's a question concerning the Ryan report, and I'll skip down to column -- line 9 on page 109, and this is your answer. "I remember except for the fact that as an internal expert I reviewed everything we did and we discuss it together" --

A I'm sorry. Which line are you talking about?

Q Yes. I'm talking about page 109, line 9.

A Okay.

Q And the question actually preceding that is "what was that work," which is referring to your work with Dr. Ryan. Your answer is "I remember except for the fact, you know, as an internal expert, I reviewed everything we did and discuss it together. I participated in two major segments of his report, the analysis of the prior art and the claim chart drawing for the pixel 306 analysis."

And then if you move on to the bottom of page 109, there's an answer where you say "the work I participated in was in the clarified function. There is a column called "clarified function," and then in the column called "structural notes." Do you see that?

A Yes, I do.

Q And it's correct you worked on the clarified function column of the claim chart that we've just been

referring to; is that correct?

A This is correct.

Q That's attached to your expert report; correct?

A Yes.

Q All right. And then if we turn to page 113 -- actually, page 112, Mr. Jacobs refers -- addresses the column we've just been referring to, and at line 11, the question is "and then you see on the right side, it says 'graphic bus and fetching logic required but not disclosed'?

"Answer: Uh-huh.

"And the quote 'required but not disclosed' refers to the graphics bus and the fetching logic?

"Answer: The graphics bus, as shown is the fetching logic, that is required, but not disclosed."

Page 113, continuing, "question: And that was a conclusion with which you agreed when this report was put together; is that correct?

"Answer: That's correct."

And then the same question and answer is read for some other similar references elsewhere in the report, and skipping over to page 119 at line 3, the question is "and that was a conclusion with which you agreed when this report was prepared?"

A Excuse me.

Q Page 114.

A 114, yes.

Q Okay. Line 3, "question: And that was a conclusion with which you agreed when this report was prepared?

"Answer: That's correct.

"Question: And you spent a lot of time with the Siann '306 since then; correct?

"Answer: Since that time?

"Question. Yes.

"Answer: Or at that time?

"Question: Since then.

"Answer: Most of the time that I spent on '306 was at that time, not since then.

"Question: Okay. You're not going to testify at trial that you disagree with the analysis in Exhibit 5 that references the elements I just read to you; correct?

"Mr. Cordell: Object to form.

"The witness: I will not disagree with it."

Do you see that?

A Yes, I do.

Q Was that the testimony you gave?

A Correct.

Q Are you telling me now you disagree with your prior answer of the Siann '306 patent?

A No, I am not.

Q So you agree that in structure shown in the Siann '306 patent, that a display memory controller, including fetch and address logic is required but not disclosed; correct?

A Could you repeat what you just said?

Q Okay. Do you agree with me that in the Siann '306 patent, a display memory controller, including fetch and address logic, is required but not disclosed by the '306 patent?

A You use the word "patent." What do you mean by the word "patent"?

Q I mean the patent.

A So do you include the claims?

Q Well, what did you mean when you were talking in your expert report?

A I meant the whole patent, including the claims.

Q That's what I'm talking about.

A Well, it is not disclosed in the specification, but it is disclosed in the claims.

Q There's a reference to a memory controller; correct?

A That is correct.

Q But it does not disclose the specifics of that memory controller; correct?

A That's correct.

Peuto, Tr. at 1373-79.

382. With respect to the Siann '306 Patent's "first means for reading the stored graphics pixels" and "second means for reading and storing the stored video pixels", Dr. Peuto opined that "a display memory controller including fetch and address logic is required but not disclosed [in the specification]." RX 616C (Peuto report), Exhibit B at S3-01980.

2. The Bindlish '864 Patent

383. U.S. Patent No. 5,608,864 ("Bindlish '864 Patent) issued on March 4, 1997 from an application filed on April 29, 1994 RX 7.

384. The Bindlish '864 Patent is related to the Nordic Product. Bril, JX 2 at 110-15; Nally, Tr. at 195.

385. Mr. Ferraro testified as follows:

> Q Isn't it true, Mr. Ferraro, that you believe that claim 37 is anticipated by the prior art of record in this case.
> A Yes, sir, that's true.
> Q And that's by the Bindlish reference; isn't that true?
> A Yes, sir, that's true.
>
> Ferraro, Tr. at 1611.

386. Mr. Ferraro acknowledged that if the Bindlish '864 Patent were deemed prior art, it would anticipate Claim 37 of the '525 Patent. Ferraro, Tr. at 1611.

387. Cirrus acknowledges that if the Bindlish '864 Patent were deemed prior art, it would anticipate Claim 37 of the '525 Patent. Cirrus Post-Hearing Brief at 93, n.18.

388. Dr. Peuto testified as follows:

> Q Does the Bindlish '864 patent disclose the video port engineering? And I'd refer you to your claim chart, and I'll give you an opportunity to retract it, because I read that part of your claim chart which does refer to some parts of the patent, but I looked at them and they're about as far removed as I could possibly see from the video port.
> A Which claim chart are you talking about?
> Q I think this is your second supplemental report, which is tab 5.
> A My second?
> Q I'm sorry, your supplemental report. I think

you'll find it at page 46 actually. Actually, if you look at claim 13, which is page 48 and 49, when it talks about the port being to memory, it refers back to 6. So let's look at what it says here as to claim 6 of the Bindlish '864 patent.

A Yes.

Q Okay. And you refer to two places as supporting a video port for receiving real-time video data and circuitry for generating an address to said memory at which said real-time video data is stored, and I guess here you just refer above, so you have these two references which I guess you assert discloses a video port into memory; correct?

A Those references allude to such a port, yes.

Q Isn't it true that this first allusion is about as general as you could possibly be. It just says we are generally interested in things like playback and live video. This doesn't tell you anything about circuitry for generating addresses.

A I would agree.

Q Now, let's look at the second one. This does talk about a memory controller, but this is talking about data, graphics and video data from the CPU, and it talks about some other source via the host bus interface. Now, that's the first port in claim 13; isn't that right?

A Yes.

Q So this does not disclose a memory address generation circuitry for a second video port, does it?

A I would have to say yes.

Q Now, you agree that the Bindlish '864 patent does not talk about a color key in the sense of an 8-bit graphics word of data that is compared to a color key; correct?

A That's my understanding.

Peuto, Tr. at 1517-18.

389. The Bindlish '864 Patent states as follows: "Since the CRT address counter in memory controller 540 counts background memory cycles, during the VW display it may count an incorrect number corresponding to the VW pixel depth. To prevent such a wrong count, the CRT address counter may be stopped while the VW is displayed and loaded with a

value corresponding to the end of the VW and restart of the background display." Bindlish '864 Patent, Column 8, lines 51-57.

390. Dr. Peuto testified as follows:

> Q Okay. And is it your testimony today that the '864 Bindlish patent teaches that, during the display of VW data, you should continue to retrieve graphics data?
> A You say the patent teaches. That sounds to me like a legal word. So what do you mean?
> Q Discloses.
> A Not in a legal sense.
> Q Well, is there disclosure? Can you point me to disclosure in the '864 patent that indicates that graphics data is retrieved while VW data is displayed?
> A I interpret the figure 3 to provide some of that basis. Figure 3 is mentioned as 3A and 3B, so it's hard to find. It's a timing diagram.
> Q What does that tell you?
> A It tells me that the way the Bindlish patent makes reference to memory is it basically fills its FIFOs, and then at the bottom you see what you see on the screen, the VW being displayed.
> Q Yes.
> A And that I expect that where the dash lines are, you continue repeating the loading of the graphics FIFOs and the video FIFOs.

Peuto, Tr. at 1511-12.

391. Dr. Peuto subsequently testified as follows:

> Q And what I see here down at the bottom right-hand corner is there's a bracketed VW. Do you see that?
> A Yes.
> Q And when I look up, I don't see happening in the CRT FIFO, VW FIFO and CRT serializer; isn't that correct?
> A You're looking up into the dashed line.
> Q Are you saying the dash line means something?
> A Generally, yes.
> Q What does it mean?
> A In this context, it means gets repeated.

Q Meaning what?
A Meaning that the CRT FIFO that you saw, the CRT FIFO, which says 40 PELS, 60 PELS, will keep on being repeated.
Q And the CRT serializer is not a dashed line, it's a solid line; correct?
A Yes.
Q That means that graphics data is not going through the CRT serializer; correct?
A No, no place, it says the CRT serializer has graphic data going through it. This is a control circuit. Data goes through a path.
Q But it's a control circuit that relates to a particular part of the graphics pipeline; correct?
A I believe so.
Q And that circuitry is not active during the VW display period; correct?
A Yes.

Peuto, Tr. at 1514-15.

392. [ ] testimony, Tr. at 97-100, concerned the Nordic Product, and not specifically the Bindlish '864 Patent. [ ]

393. [ ] testimony regarding "always rastering" lacks clarity, and is unreliable. [ ]

394. The '525 Patent, in its entirety, does not suggest a distinction between "to" the pipeline and "through" the pipeline. CX 1.

395. The specification of the Bindlish '864 Patent includes a statement that "the data pipeline is kept full." RX 7, Column 10, line 38.

396. The specification of the Bindlish '864 Patent indicates that the CRT address counter may be stopped. RX 7, Column 8, lines 54-57.

E. <u>Section 102(g) – Invented by Others</u>

397. See previous findings of fact regarding Oak/Brooktree, *infra*.

F. Section 102(f) – Derivation of Invention

398. ATI withdrew this invalidity defense. ATI Post-Hearing Brief at 108.

G. Section 103

399. Mr. Ferraro opined that a person of ordinary skill in the art at the time of the '525 Patent " would have been schooled in electrical engineering, would have two years of experience in digital circuitry design and would have sufficient systems knowledge so as to understand the block diagram of Figure 2 of the '525 Patent. Such a person would be versed in PC graphics, have some knowledge of video processing, but not necessarily have direct graphics or video controller chip design experience." CX 745C at 75 (Ferraro Rebuttal Report).

400. Mr. Ferraro opined:

> The overall contribution of an architecture lies in its unique design. In this respect, the value of the '525 patent is much greater than the sum of its individual parts. The interrelationship between circuit elements in an architecture determines its performance. One cannot necessarily add or subtract from a design without adversely affecting its performance. This is true for all architectural systems, the '525 and other prior art designs included. Dr. Peuto's implicit approach – searching for whether the individual elements were present in the prior art – if adopted, would invalidate virtually any patent on an architecture.
>
> CX 745C at 75 (Ferraro Rebuttal Report).

401. At the hearing, when questioned on cross-examination, ATI's expert, Dr. Peuto, was not prepared to give testimony regarding the teachings of the Romesburg '643 Patent. Peuto, Tr. at 1411-12.

402. Cirrus manufactured and sold the Cirrus Pixel CL-PX2070/CL-PX2080 and its upgrade,

the 2085 (collectively "2070/2080") prior to January 23, 1995. Schafer, Tr. at 640; RX 304, RX305.

403. Mr. Schafer testified as follows:

> Q And we're back to the 2070/2080. Isn't it true that the 2070/2080 products were sampled as a chip set around the fourth quarter of 1992?
> A That sounds right.
> Q And for the record, we're referring to RX-295. Isn't it true that the terms "sampling" within Cirrus includes delivery of chips to customers?
> A Yes.

Schafer, Tr. at 640.

404. The 2070/2080 consisted of several components that were designed and sold as a combination product. Schafer, Tr. at 628.

405. The 2070/2080 lacks a unified frame buffer, lacks the dual FIFOs described in Claims 16, 17, and 23, and does not perform vertical interpolation as set forth in Claim 23. ATI Post-Hearing Brief at 111-12.

406. The 2070/2080 had two separate frame buffers, one for graphics and one for video. Schafer, Tr. at 643; Ferraro, Tr. at 1571.

407. Mr. Nally testified that a unified frame buffer was desired by customers for cost savings and was a goal of the VESA Media Channel, an industry standards group. Nally, Tr. at 202, 204.

408. In his written expert report, Dr. Peuto stated in a conclusory fashion that implementation of a unified frame buffer for the two separate frame buffers in the 2070/2080 would have been obvious to one of skill in the art at the time of the '525 Patent invention. RX 618C

at 82.

409. Dr. Peuto offered no live testimony regarding the obviousness of substituting a unified frame buffer for the two separate frame buffers in the 2070/2080.

410. Mr. Ferraro testified as follows:

> Q And to come back to your obviousness discussion at the beginning, why wouldn't it have been obvious to compress those two separate frame buffers into a single frame buffer?
>
> A If you see the chain of events that led to the last row of my chart, all of that evolution of product had to take place to get from that dual frame buffer to the single frame buffer with the claim element. So it was not a simple -- it was not a simple thing to retrieve both graphics or video or to know how to do it and all that. So it's far from obvious.
>
> Q So you're pointing to sort of the great leap forward necessary to go from the pixel frame -- dual frame buffer approach to the '525 single frame buffer approach?
>
> A Yes.
>
> Q And that's sort of an empirical -- I guess that's an empirical basis for making an obvious determination, but from the technical engineering standpoint, why would it have been hard, with respect to the pixel products, to simply compress them into a single frame buffer?
>
> A Well, to have a single frame buffer, you'd have to have a single controller, and I don't think that they had the -- I don't think that it would have been obvious to someone picking up these two single controllers how to actually combine them and put it together. I mean, a lot of engineering would have been involved. And was involved.

Ferraro, Tr. at 1573-74.

411. Mr. Ferraro's expert testimony regarding the obviousness of substituting a unified frame buffer for two separate frame buffers is more credible and convincing than Dr. Peuto's expert testimony on this issue.

H. Section 112, ¶ 2

412. See Findings of Fact, *supra*, regarding indefiniteness of claim limitations.

I. Section 112, ¶ 1 - Written Description

413. ATI's pre-hearing brief failed to address this issue.

J. Section 112, ¶ 1 - Enablement

414. See Findings of Fact, *supra*, regarding indefiniteness of claim limitations.

K. Section 112, ¶ 1 - Best Mode

415. Mr. Nally testified as follows:

> Q I would like to get back to the FIFOs for a moment, if I can. You told me at your deposition that the small FIFOs were very important; correct?
> A Yes.
> Q And part of the reason why you said they were so important is that -- well, was that they were an advantage you realized by being able to grab small chunks of the data in each memory cycle; correct?
> A There was probably a miscommunication there. To grab small chunks of data. It allowed us to have a small FIFO.
> Q But the two are related; right?
> A Yes.
> Q So the small FIFO was the advantage you realized out of being able to grab the small chunks of data?
> A Yes.
> Q The idea in the '525 patent is that you don't have to go out and retrieve an entire line of data before displaying that line on the screen; correct?
> A A large portion -- you don't necessarily have to store the whole line but you've got to store a lot of data.
> Q But your chunk I, if we can call that, memory retrieval scheme allows you to get less than a full line? That is absolutely true isn't it?
> A Yes.
> Q That's a big advantage of the invention, isn't it?
> A Yes.

Q One of those advantages you pointed out is you don't need as big a FIFO; correct?

A Correct.

Q Now, doesn't that also mean that your FIFO has to continuously process data as each small chunk is fed into the input port of that FIFO?

A Only if the pipeline high-end FIFO is run.

Q I see. Good point. But in the case where the video pipeline is moving, is active, the video data is being displayed on the screen, that small FIFO needs to keep moving data through it at all times; correct?

A That is correct.

Q The FIFO will be emanating from the video -- strike that.

The video data will be emanating from the FIFO at at least the rate that it's being displayed on the CRT; correct?

A Not necessarily.

Q That's because you may have scaling downstream in the FIFO?

A Yeah. If you've got scaling going on, the rate of data coming out of FIFO does not match the rate of data going to the display screen.

Q Thought about it as soon as it left my mouth. You're exactly right. There may be the case where there's scaling. Let's take the case where there's no scaling, and that does happen?

A Right.

Q In the case where there's no scaling, the data is leaving the FIFO at [sic] at least the display rate of the CRT?

A Correct.

Q And that means that data has to be placed into the FIFO at at least that same rate; correct?

A That's correct.

Q So you continuously feed the small FIFO and continuously throw data out as long as the video pipeline is there?

A The difference is the back end is a steady stream. The front end is a chunkier, a burst scheme.

Q So we've got a bursting retrieval out of the memory into the small FIFO and the data is moving continuously through that FIFO and emanating at a regular rate?

A Correct.

Q And the interpolation scheme of the '525 patent takes data in word-sized units out of the FIFOs and then interpolates them word by word; correct?

A I believe so.

Q So the minimum burst of data that is retrieved in the '525 patent is a word data; correct?

A We treat the burst as a number of 32-bit increments. Okay? It might be four blocks of 32. It might be eight blocks of 32.

Q The idea is that it's some number -- some integral number of words that you're pulling out of memory with each burst; correct?

A Yes.

Q The idea behind the '525 patent, the thing that gives you these great advantages is you're able to take those bursts in very small chunks?

A Correct.

Nally, Tr. at 156-60.

416. Mr. Nally testified as follows:

Q Let's talk a little bit more about the small FIFO issue that we discussed back in your deposition. You thought that was a pretty good feature, didn't you?

A Yes, I did.

Q In fact, you characterized it as exciting; isn't that true?

A Yes.

Q But you didn't tell the Patent Office that this was an exciting feature, did you?

A I'm glad to say that what I thought I had to reveal to the Patent Office was what was unique and different, and what was really unique and different was the cycle stealing mechanism to allow me to have the small FIFOs. The small FIFOs was an achievement. It wasn't the -- what's the word I'm looking for here. It was the benefit of the real invention.

Q It was the advantage?

A It was the advantage. That's why I say it was the benefit of the invention. It gave me a real edge over my competitor.

Q You didn't tell the Patent Office this was the benefit of the invention, did you?

A No, I didn't think it had any bearing over the patent at all. I was supposed to disclose what the invention did, and I didn't think it was part of my job to do the marketing -- to say that -- engineering is engineering, marketing is marketing. I wear two hats The marketing side of the architect saw an exciting feature. The engineering side of it saw something that had to be -- that was okay, this is something that I've got to explain to the Patent Office. What I'm doing. What I explained to the Patent Office is what I'm doing, and the marketing side is really excited because they're getting this feature and that feature is cycle stealing.

Q Earlier in your testimony today, I thought I heard you characterize a different feature as the key to the invention and that was the ability to put a video window on the screen under register control. Do you recall that?

A Yes.

Q Did you mean to say that that was a key to the invention?

A There's a number of key -- this is a system of architect, okay. A lot of things we did were key. If either one of these things was missing, we were going to probably be in the same boat as everybody else in the industry. We would have probably had a product that was almost good enough. So yeah, all these things to me were key, and every one of them had to be there.

Q Well, and you also said that you didn't see this in the prior art, this ability to position a video window under register control; isn't that right?

A Yeah, because everything I knew existed at the time was using mask tags.

Q And you also said that you were unaware of anyone else in the prior art providing for Y interpolations; isn't that true?

A That is true.

Nally, Tr. at 136-39.

IV. Enforceability

417. On May 2, 1995, the applicants filed a first Information Disclosure Statement identifying

the following eight prior art patents, all of which were cited earlier during the prosecution of a co-pending application (No. 08/098/846) that was incorporated by reference in the '525 Patent application: 5,257,348 (Roskowski *et al.*), 5,274,753 (Roskowski *et al.*), 5,229,852 (Maietta et ai.), 5,341,318 (Balkanski et al.), 4,991,122 (Sanders), 5,365,278 (Willis), 5,341,442 (Barrett), and 5,218,432 (Wakeland). CX 2 at 143-47.

418. On January 17, 1996, the examiner issued a first Office Action rejecting the claims of the '525 patent application on the grounds that the claims were obvious in light of one or more of the following articles: (1) EDGE: Work-Group Computing Report, October 3, 1994, v5; (2) Jeff Mace "Mainstream Graphics Accelerators Rush Power," PC Magazine, Dec. 1994, v13; (3) Anthony Cataldo "WD, Cirrus Show Video Playback ICs," Electronic News, Oct. 1994, v40; and (4) Dave Bursky "Acceleration Puts the "Snap" into Graphics," Electronic Design, July 1994, v42. CX 2 at 151-59.

419. The examiner did not mention any particular products in the first Office Action. CX 2 at 151-59.

420. The articles the examiner cited report on the features of numerous products, including the Cirrus CL-GD5440 and CL-GD7542 products. CX 2; CX 26; CX 27; CX 28; CX 29

421. Mr. Nally and Mr. Schafer designed the CL-GD5440 product. Schafer, Tr. 569.

422. The applicants responded to the first Office Action in their remarks following the Amendment Transmittal dated February 5, 1996, and in the supporting declarations of Mr. Nally and Mr. Schafer. CX 2 at 165-77

423. On February 5, 1996, the applicants submitted a second Information Disclosure Statement identifying U.S. Patent No. 5,406,306, the Siann '306 Patent. CX 2 at 161-63.

424 The second Information Disclosure Statement included the following statement:

> The '306 patent is directed to the same general problem as is the invention disclosed in the above-identified patent application but deals with the problem in a different manner. In the '306 patent there is also a single memory for storing both graphics and video data. However, in the '306 patent the data is divided according to graphics or video with each being stored in a different portion of the memory. The data is then treated separately throughout the circuit. For example, the video data is processed at one frequency and the graphics data is processed at a different frequency. It is only when the two different data forms are actually sent to the monitor are they both processed at the same frequency. The '306 specification primarily deals with the concept of handling the processing of the different data forms (video and graphic) using different frequencies and does not, in any manner, deal with or even hint at the concept of dividing the data into on-screen and off-screen portions. Neither does the '306 patent deal with or even hint at 1) dividing the single memory into on-screen and off-screen portions, or 2) providing the on-screen and off-screen portions to the screen under control of different pipelines, as is specifically claimed in the invention in the above-identified application.

CX 2 at 162 (emphasis in original).

425. Mr. Nally testified that when he analyzed the Siann '306 Patent during the prosecution of the '525 Patent, he believed that the dotted line in Figure 3 of the Siann '306 Patent indicated that the Siann '306 Patent uses a split frame buffer, that is, a frame buffer in which half of the frame buffer is used for video and half is used for graphics. Nally, Tr. 106.

426. Mr. Nally testified that during the prosecution of the '525 Patent, he believed that the Siann '306 Patent involved a hard partition between video and graphics in its frame buffer, similar to schemes in which video data and graphics data were stored in entirely separate frame buffers. Nally, Tr. 107.

427. The text of the Siann '306 Patent does not contain the phrases "on-screen" or "off-screen". CX 157; Peuto, Tr. 1299.

428. Mr. Schafer's current understanding of the specification of the Siann '306 Patent is that it does suggest dividing a single frame buffer into on-screen and off-screen portions. Schafer, Tr. 631-32.

429. Mr. Nally now believes that part of the Siann '306 Patent specification describes dividing video and graphics data in a single frame buffer such that it could be interpreted as describing a memory having on-screen and off-screen areas. Nally, Tr. 214.

430. The concept of on-screen and off-screen memory is distinct from the concept of dividing memory into video and graphics portions. Ferraro, Tr. 504-08.

431. The examiner had the Siann '306 Patent before him when he evaluated the second Information Disclosure Statement, and for the remainder of the prosecution of the '525 Patent. CX 2 at 161-64.

432. In the first Office Action mailed January 17, 1996, the examiner referred to the concepts of on-screen and off-screen memory, even where those exact phrases had not been used, because he stated: "EDGE discloses that Cirrus Logic's MotionVideo Architecture includes a multi-format buffer that stores YUV signals from a video stream and RGB format from a computer (pg. 1). EDGE does not expressly disclose writing data to on-screen and off-screen memory of the frame buffer. However on-screen and off-screen memories are well known and common in the art and Mace teaches using off-screen memory to change resolution and color depth of the video." CX 2 at 153.

433. The Siann '306 Patent is one of the closest prior art references that has been presented in

the case. CX 745C at 78-79 (Ferraro Rebuttal Report)

434. Mr. Nally testified that he believes, and believed during the prosecution of the '525 Patent, that he was not required to disclose the Siann '306 Patent to the Patent Office because he believed that the Siann '306 Patent, being a two- or three-chip solution instead of the one-chip solution of the '525 Patent, was not significant prior art. Nally, Tr. 184.

435. [

]

436. [

]

437. [

]

438. [

]

439. Mr. Siann indicated that the Brooktree Bt885 "implemented some [but not all] of the particular circuitry as defined by the ['306] patent," and Mr. Ferraro therefore opined that it is therefore a cumulative reference because the applicants disclosed the Siann '306 Patent. CX 745C at 79 (Ferraro Rebuttal Report); see also Siann, Tr. 1041-42.

440. Mr. Nally testified that he believed, during the prosecution of the '525 Patent, that the 2070/2080 was not significant prior art because it is a two- or three-chip solution, not the one-chip solution of the '525 Patent. Nally, Tr. 184.

441. Mr. Nally and Mr. Schafer did not disclose the CL-GD5430 because it was a graphics-only device, and they believed it was not relevant to the '525 Patent. Schafer, Tr. 599-600.

442. Mr. Nally testified that he did not disclose the Intel i750/DVI because he did not believe (and does not believe) that it is related to the '525 Patent. Nally, Tr. 184-85.

443. During the prosecution of the '525 Patent, Mr. Schafer had heard of the Intel i750 product, but did not know about its functionality, and does not recall reviewing any detailed specification of that product. Schafer, Tr. 597.

444. Mr. Nally testified that he believed, during the prosecution of the '525 Patent, that he was not required to disclose the 2070/2080 to the Patent Office because it was not significant to the '525 Patent. Nally, Tr. 184.

445. Mr. Nally testified that he believed, during the prosecution of the '525 Patent, that the Nordic product and the Bindlish '864 Patent were directed toward a technique for compressing video, and did not have anything to do with the '525 Patent. Nally, Tr. at 112-13.

446. Mr. Schafer testified that he did not disclose the Nordic product to the Patent Office because "the only features [he] was aware of on Nordic that were unique were very flat panel specific, and [he] didn't feel that that applied to the '525" Patent. Mr. Schafer also thought that anything in the Nordic CL-GD7542 relevant to the '525 Patent was

something that the CL-GD5440 team provided to the Nordic team, and therefore was something that Mr. Nally and Mr. Schafer invented. Schafer, Tr at 593.

447 [

]

Conclusions of Law

1. All conclusions of law set forth in the opinion are incorporated herein by reference.

2. The U.S. International Trade Commission has personal jurisdiction over the parties and subject matter jurisdiction over this investigation.

3. ATI has imported and sold the accused products, the ATI Rage Devices.

4. The evidence proffered by Cirrus fails to demonstrate satisfaction of the domestic industry requirement of Section 337.

5. The evidence of record demonstrates that Claims 13, 15, 16, 17, 23 and 37 of the '525 Patent are invalid.

6. Even assuming, *arguendo*, the validity of Claims 13, 15, 16, 17, 23 and 37 of the '525 Patent, the evidence of record does not demonstrate that the ATI Rage Devices infringe these claims.

7. There is no violation of Section 337 with respect to the ATI Rage Devices and the '525 Patent.

INITIAL DETERMINATION AND ORDER

Based on the foregoing opinion, findings of facts, conclusions of law, and the record as a whole, and having considered all pleadings and arguments as well as proposed findings of fact and conclusions of law, it is my Initial Determination ("ID") that no violation of Section 337 exists in the importation into the United States, sale for importation, or sale within the United States of certain video graphics display controllers and products containing same.

I hereby certify to the Commission this ID, together with the record of the hearing in this investigation consisting of the following:

I. The transcript of the prehearing conference held on September 16, 1998, and the transcript of the hearing held from January 21, 1999 to January 29, 1999,

II. The exhibits accepted into evidence in this investigation as listed in the attached exhibit lists, and

III. All orders entered in this investigation as well as all pleadings, briefs and other documents and things filed with the Secretary.

In accordance with 19 C.F.R. § 210.39(c), all confidential material under 19 C.F.R. § 210.5 is to be given *in camera* treatment.

The Secretary shall serve a public version of this ID upon all parties of record and the confidential version upon counsel who are signatories to the Protective Order (Order No. 1) issued in this investigation, and the Commission investigative attorney. To expedite service of the public version, counsel are hereby Ordered to serve on my office no later than May 10, 1999, a copy of this ID with those sections considered by the party to be confidential bracketed

in red.

Pursuant to 19 C.F.R. § 210.42(h), this ID shall become the determination of the Commission unless a party files a petition for review pursuant to § 210.43(a) or the Commission, pursuant to § 210.44, orders on its own motion a review of the ID or certain issues herein.

Debra Morriss
Administrative Law Judge

Issued:

Exhibit List of the Administrative Law Judge
Inv. No. 337-TA-412

Exhibit Number	Description of Exhibit
ALJ Ex. 1	Transcript, including demonstrative aids, of Tutorial Session held on January 7, 1999

FINDINGS OF FACT and CONCLUSIONS OF LAW
TABLE OF CONTENTS

Findings of Fact

Background

1. All findings of fact set forth in the opinion are incorporated herein by reference.

2. The Complainant in this investigation is Cirrus Logic, Inc. ("Cirrus"), a California corporation. Notice of Investigation.

3. The Respondent in this investigation is ATI Technologies, Inc. ("ATI"), a Canadian corporation. Notice of Investigation; ATI's Response to the Complaint, ¶ 5.

4. Cirrus filed a complaint against ATI under 19 U.S.C. § 1337 ("Section 337") based on the alleged importation into the United States, the sale for importation, and the sale within the United States after importation of certain video graphics display controllers and products containing same. Complaint.

5. The accused products are ATI's Rage Pro, Rage Pro LT and Rage 128 (collectively, "Rage Products" or "Rage Devices"). Cirrus Pre-Hearing Brief at 12.

6. The Commission issued its notice of investigation on July 28, 1998, instituting this Section 337 investigation concerning Cirrus' allegations of ATI's infringement of claims 37 and 43 of United States Patent No. 5,598,525 ("the '525 Patent") owned by Cirrus, as well as Cirrus' claim of the requisite domestic industry. The Commission named Cirrus as the Complainant, and ATI as the sole Respondent in this investigation. Notice of Investigation.

7. The notice of investigation in this matter was amended to add certain other claims, and later amended to delete certain claims, and ultimately the hearing in this investigation concerned alleged infringement of only claims 13, 15, 16, 17, 23 and 37 of the '525

Patent. Notice of Investigation; Cirrus Notice of Withdrawal of Certain Claims.

8. The '525 Patent is entitled "Apparatus, Systems and Methods for Controlling Graphics and Video Data in Multimedia Data Processing and Display Systems," and was issued on January 28, 1997. CX 1.

9. The invention disclosed in the '525 Patent is directed to an apparatus designed to provide for the flexible control of graphics and video data in a display control environment. CX 1, Column 2 lines 41-43.

10. The named inventors of the '525 Patent are Messrs. Robert M. Nally and John C. Schafer. CX 1

11. The named inventors assigned the invention to Cirrus Logic, Inc. CX 1.

12. The application that issued as the '525 Patent was filed on January 23, 1995. Thus, the "critical date" (*i.e.* the date one year prior to the filing date) of the '525 Patent is January 23, 1994. CX 1; 35 U.S.C. § 102(b).

13. The hearing in this matter commenced on January 21, 1999, and concluded on January 29, 1999. All parties were represented at the hearing.

I. Jurisdiction

A. Importation

14. ATI imports into the United States the Rage Products. Stipulation by ATI; See ATI Post-Hearing Brief at 6.

B. Domestic Industry

1. Economic Prong

15. MiCRUS is a manufacturing joint venture between Cirrus and IBM which was formed in

1994 and which produces wafers for both companies. Baker, Tr. at 436; CX 493 at CL 51288; CX 494 at 142598.

16. The MiCRUS facility, also known as fab A, is located in East Fishkill, New York. Baker, Tr. at 436; CX 493 at CL 51288; CX 494 at CL 142598.

17. As of the date of the trial, Cirrus owned 48 percent of MiCRUS, a percentage which has been unchanged over the past year. Parsons, Tr. at 454-55; CX 494 at CL 142598.

18. [ ] CX 488.

19. All of the Laguna 5465 ("5465") products sold by Cirrus have been manufactured at MiCRUS. Baker, Tr. at 435-36; CX 481C at CL 41265-266.

20. Products manufactured at the MiCRUS facility are marked on the top side brand of the device with the letter indicating the MiCRUS fab so customers are aware of where their products were manufactured. Baker, Tr. at 436.

21. In 1997, the total number of wafers for the 5465 product (also known as Laguna 3DAGP) shipped from MiCRUS to Cirrus was [ ] Parsons, Tr. at 460-62; CX 520C at CL 128329.

22. From January through June, 1998, the total number of wafers for the 5465 product shipped from MiCRUS to Cirrus was [ ] CX 520C at CL 128331.

23. Cirrus' investments in MiCRUS include equity in the joint venture, manufacturing payments, equipment, and facilities improvements. Parsons, Tr. at 455; CX 493 at CL 51289.

24. The amount of Cirrus' equity investment in MiCRUS totaled $23.8 million. Parsons, Tr. at 457; CX 493 at CL 51289.

25. Cirrus' manufacturing payments relating to MiCRUS are payments for access to IBM's process technology. Parsons, Tr. at 455.

26. The amount of Cirrus' investment in the MiCRUS joint venture through manufacturing payments totals $71 million. Parsons, Tr. at 457; CX 493 at CL 51289.

27. Cirrus' investment in improvements to the MiCRUS facilities represents investment in improving the physical building, environment, chemical distribution, heating, ventilation and cooling. Parsons, Tr. at 456.

28. The amount of Cirrus' investment in MiCRUS facilities improvements totals $29.7 million. Parsons, Tr. at 458; CX 493 at CL 51289.

29. Cirrus' previous investment in equipment represents guarantees on leases on the MiCRUS fabrication equipment. Parsons, Tr. at 456.

30. The amount of Cirrus' previous investment in MiCRUS equipment is $360 million. Parsons, Tr. at 458; CX 493 at CL 51289.

31. Cirrus researched and developed the 5465 product in the United States. Baker, Tr. at 437-438.

32. The first commercial shipment of the 5465 was in April, 1997. Baker, Tr. at 438.

33. Research and development activities for the 5465 did not end at the time of the first commercial shipment of the product. Baker, Tr. at 438.

34. Research and development activities on the 5465 that continued after April, 1997, include software development and maintenance for the product, and maintenance and functionality improvement to the drivers. Baker, Tr. at 438.

35. Cirrus has attempted to license its graphics portfolio, including the '525 Patent, to [

] JX 5C at 41-42 (Donohue Dep. Tr.); CX 144, 147, 648, 649.

36. Cirrus has licensed the '525 patent to [ ] JX 5 at 72 (Donohue Dep. Tr.); CX 128.

37. Under the license agreement with [ ] which included the '525 Patent, Cirrus received monetary consideration of [ ] JX 5 at 75 (Donohue Dep. Tr.).

38. Mr. Kyle Baker, an employee of Cirrus Logic, testified that he was familiar with Cirrus revenues for its video graphics display products in the first quarter of fiscal year 1999 and that the 5465 produced the most revenue. Baker, Tr. at 431.

39. Revenues for the 5465 product in fiscal year 1998 were over [ ] CX 623C at CL 122052.

40. The first quarter for Cirrus' fiscal year 1999 begins April 1st of 1998 and runs through the end of June of 1998. The approximate revenues from the 5465 product for that quarter were about [ ] Baker, Tr. at 431.

41. Cirrus has not stopped offering for sale the 5465 product. Baker, Tr. at 432.

42. If orders accepted for the 5465 product exceed existing inventory, additional wafers would be started at the MiCRUS facility. The MiCRUS facility is currently operating at this time. Baker, Tr. at 435.

43. Approximately [ ] units of the 5465 product are in Cirrus' inventory. These products are in die form, to be packaged, and must be tested before they are ready for customer shipping. Baker, Tr. at 433.

44. Testing of the 5465 products occurs at Cirrus' Fremont facility by using an HP tester. The cost of an HP tester is estimated to be around [ ] Baker, Tr. at 433-34.

45. Current research and development activities have been contracted out to and are being

conducted by ISD Corporation in San Jose, California on behalf of Cirrus. The work began in November of 1998. Cirrus has paid out to ISD Corporation approximately [ ] for work that includes maintenance and development on the 5465 product. The [ ] already paid is reflected in the contract between Cirrus and ISD under [ ] Baker, Tr. at 439-441, 451; CX 485 C at CL 115124.

46. Cirrus expects to pay at least [ ] in the future to ISD under their contractual obligation for work done. Baker, Tr. at 440.

47. Cirrus admits that it has redeployed "its business away from PC display products." Cirrus Pre-Hearing Brief at 7.

48. Cirrus admits that it has been [ ] the 5465 chip. Baker, Tr. at 450.

49. Cirrus admits its sales revenues from the 5465 are in decline. Baker, Tr. at 432.

2. Technical Prong

50. Mr. Ferraro indicated that in connection with forming his expert opinions, he reviewed, *inter alia*, the CL GD 5465 Preliminary Data Book, Version 2.0, the CL GD 5465 Visual Media 3D Graphics Accelerator Data Sheet, the CL GD 5465 Preliminary Product Bulletin, the CL GD 5465 Technical Reference Manual, the Laguna 3DA specification, the deposition transcripts of Mr. John Schafer and the deposition transcript of Mr. Robert Nally. CX 745C at 3 (Ferraro Expert Report).

51. Cirrus' 5465 is a controller. CX61C; CX62C. .

52. The 5465 has circuitry that selects between on-screen and off-screen memory as it writes video and graphics data into the frame buffer. Schafer, Tr. at 584; CX 61C at CL 88352,

CL88354; CX 745C at 99-101 (Ferraro Supplemental Report).

53. Mr. Schafer participated in the development of the 5465. Schafer, Tr. at 581, 591.

54. Mr. Schafer testified that 5465 controller utilizes address data to determine where in the frame buffer data is written. Schafer, Tr. at 584.

55. The 5465 has a memory controller that writes graphics pixel data into the on-screen buffer and video data into the off-screen buffer in the frame buffer memory. CX 61C at CL 88352, CL88354; CX 745C at 99-101 (Ferraro Supplemental Report).

56. The 5465 has a frame buffer divided into on-screen and off-screen areas. Schafer, Tr. at 582-83.

57. The 5465's frame buffer stores graphics data in its on-screen area and video data in its off-screen area. CX 62C at CL89104-05; CFF 89.

58. The 5465 does not store video data in its YUV format in the on-screen area of the frame buffer. Keene, JX 11C at 155.

59. The 5465 has a host bus interface that accepts video or graphics data, directing the data to the appropriate memory storage location according to the address. Schafer, Tr. at 583-84.

60. In the 5465, the addresses accompanying words of data determine in what area of the frame buffer the data should be written. Data in the on-screen area is processed as graphics, and data in the off-screen area is typically processed as video. CX 745C at 99-101; Schafer, Tr. at 584-85.

61. Mr. Ferraro opined that the 5465 has a V-port for receiving real-time video data. CX 745C at 99-101.

62. Mr. Schafer testified that the 5465 has a video interface for connection to a real-time

video source. Schafer, Tr. at 587.

63. The 5465 has the "second port" described in Claim 13. CX 745C at 99-101; Schafer, Tr. at 587-89; CX 62C.

64. Mr. Schafer testified that the 5465 generates addresses for the real-time video data received through the video port, and these addresses are provided to the memory controller. Schafer, Tr. at 588-89.

65. Mr. Schafer testified as follows:

> Q Let's turn into tab 12 towards the back again, page 16-20. It's in the video programming note section. In the first paragraph, I'm going to read you a few sentences starting with the third sentence. "At the beginning of each scan line, pixels are fetched and displayed from the background data source until VW_HSTRT pixels have been displayed. Then pixels are fetched and displayed from the window data source until VW_HEND pixels have been displayed. This is the window area. If occlusion is being used, pixels are fetched from both sources so that either the background or window can be displayed."
>
> Can you describe for us the retrieval of data from the frame buffer with the 5465?
>
> A The 5465, in general, would raster data from the frame buffer for the graphics display for the entire scan line. So all of the graphics data for a particular line was fetched. As far as video data goes, that would only be fetched during the -- for the portion of screen that had a video window display, as indicated by these lines you just read to me.
>
> Q You said during the scan line. Does that mean that the 5465 would retrieve both types of data during the actual raster of the screen?
>
> A There was actually a mechanism for prefetching data at the beginning of a line to fill the graphics and video FIFOs, and then once the active graphics display started, the graphics pipe would be depleted, data would be transferred into that as needed to keep that FIFO full. It wouldn't be until the video window started that the video

data would be displayed and depleting that FIFO. At that time, video data would be fetched.

So for the duration of the video window, both video and graphics data were being fetched from the frame buffer. Once the video window was completed, then it would go back to just fetching graphics data.

Schafer, Tr. at 589-90.

66. The 5465 has circuitry for selectively retrieving video or graphics data from the on-screen and off-screen areas during rastering. Schafer, Tr. at 589-90; CX 745 C at 99-101.

67. Mr. Ferraro indicated that the 5465 meets the "graphics backend pipeline" and "video backend pipeline" limitations of Claim 13. CX 745C at 99-101.

68. Mr. Schafer testified that the 5465 contains a graphics backend pipeline that processes for display data retrieved from the frame buffer. Schafer, Tr. at 585.

69. Mr. Schafer testified that the 5465 contains a video backend pipeline that processes for display video data retrieved from the frame buffer. Schafer, Tr. at 585

70. Mr. Schafer testified that the graphics and video pipelines in the 5465 are separate pipelines. Schafer, Tr. at 586-87.

71. Mr. Schafer did not give inconsistent testimony regarding the separate pipelines in the 5465. Schafer, Tr. at 586-87.

72. Cirrus product information in the 5465 includes the statement that "If occlusion is being used, pixels are fetched from both sources [on-screen and off-screen] so that either the background or window can be displayed." CX 62C at CL 89103.

73. Mr. Schafer testified as follows:

Q You said during the scan line. Does that mean that the 5465 would retrieve both types of data during the

A There was actually a mechanism for prefetching data at the beginning of a line to fill the graphics and video FIFOs, and then once the active graphics display started, the graphics pipeline would be depleted, data would be transferred into that as needed to keep that FIFO full. It wouldn't be until the video window started that the video data would be displayed and depleting that FIFO. At that time, video data would be fetched.

So for the duration of the video window, both video and graphics data were being fetched from the frame buffer. Once the video window was completed, then it would go back to just fetching graphics data.

Schafer, Tr. at 590.

74. The 5465 can operate in an occlusion mode where on-screen graphics pixels are rastered out for every pixel location on the display monitor, but these graphics pixels can be overlaid and occluded by other pixels, with the 5465's multiplexer selecting on a pixel-by-pixel basis between video and graphics. Schafer, Tr. at 590; CX 62C at 89103, 89106.

[illegible]ing of graphics data in the 5465 is ongoing, regardless of the display of a video [illegible]see Schafer, Tr. at 590; CX 62C at 89103, 89106.

[illegible]5. The 5465 "pre-fetches" video data by retrieving it from the frame buffer and storing it in a FIFO in the video pipeline prior to the display raster scan reaching a display position of a window. The pre-fetched video data is held in the FIFO until it is needed for display. Schafer, Tr. at 590.

77. In the 5465, video data is rastered to the video backend pipeline before the display raster scan reaches a display position of a window. Schafer, Tr. at 590.

78. It is not possible to apply the "when" limitation of Claim 13 to the 5465's process of rastering video data to the video backend pipeline because of the limitation's indefinite

nature.

79. The 5465 contains a multiplexer controlled by a circuit that uses video window position information as well as color keying to determine for each pixel location whether video or graphics data will be passed. Schafer, Tr. at 582, 591.

II. Infringement

A. Claim Construction

1. Claims 13 and 37

80. Claim 37 of the '525 Patent reads as follows:

37. A display controller comprising:

circuitry for selectively retrieving data from an associated multi-format frame buffer for simultaneously s[t]oring graphics and video data;

a first pipeline for processing words of graphics data selectively retrieved from said frame buffer; and

a second pipeline for processing words of video data selectively retrieved from said frame buffer.

CX 1

81. Claim 13 of the '525 Patent reads as follows:

13. A controller comprising:

circuitry for writing selectively each word of received data into s [a] selected one of on-screen and off-screen memory spaces of a frame buffer;

a first port for receiving video and graphics data, a word of said data received with an address of said memory spaces directing said word to be processed as a word of video data or a word of graphics data;

a second port for receiving real-time video data;

circuitry for generating an address associated with a selected one of said memory spaces

for a word of said real-time video data;

circuitry for selectively retrieving said words of data from said on-screen and off-screen memory spaces as data is rastered for driving a display;

a graphics backend pipeline for processing ones of said words of data representing graphics data retrieved from said frame buffer;

a video backend pipeline for processing other ones of said words of data representing video data retrieved from said frame buffer, said circuitry for retrieving always rastering a stream of data from said frame buffer to said graphics backend pipeline and rastering video data to said video backend pipeline when a display raster scan reaches a display position of a window; and

output selector circuitry for selecting for output between words of data output from said graphics backend pipeline and words of data output from said video backend pipeline.

CX 1.

82. The phrase "a controller" found in Claims 13 and 37 gives meaning and context to these claims.

83. The phrase "a controller" does not require a single, integrated circuit controller design or a single chip. Ferraro, Tr. at 1632.

84. The '525 Patent makes no mention of a "single integrated circuit" or a single chip. See CX 1.

85. Other Cirrus patents set forth a single chip limitation in plain terms. See e.g, Cirrus '573 patent (RX-90) ("A processing device disposed on a single chip comprising"); Cirrus' '270 patent (RX-91) ("wherein said processing ...and said first and second memory banks are fabricated on a single, integrated circuit chip"); Cirrus '279 patent (RX-611) ("A monolithic integrated circuit comprising").

86. Cirrus' expert Mr. Ferraro testified as follows: "I haven't abandoned the contention that is

not a single chip, but I have abandoned - I do not stand behind that statement in my expert report where I would distinguish a piece of prior art merely because it was on one integrated it was on one integrated [sic] circuit and not another integrated circuit." Ferraro, Tr. 1632.

87. The dotted line in Figure 2 of the '525 Patent shows the relationship between what is shown in that figure and what is shown in Figure 1 of the '525 Patent. See CX 1.

88. "Word" in the '525 Patent refers to a unit of data. Ferraro, CX 745C at 7; Peuto, ALJ1 at 102.

89. Figure 1 of the '525 Patent shows the frame buffer 107 as a separate element from the controller 105. CX 1, Figure 1; CX 1, Column 4, line 61 - Column 5, line 9.

90. The '525 Patent states:

> Frame buffer memory 107 provides temporary storage of the graphics and video data during processing prior to display on display unit 106. According to the principles of the present invention, VGA controller is operable in selected modes to store graphics and video data together in frame buffer 107 in their native formats. In a preferred embodiment, the frame buffer area is partitioned into on-screen memory and off-screen memory. Frame buffer 107 is also a "unified" memory in which video or graphics data can be stored in either the on-screen or off-screen areas. In the preferred embodiment, display unit 106 is a conventional raster scan display device and frame buffer 107 is constructed from dynamic random access memory devices (DRAMs).
>
> CX 1, Column 5, lines 25-38.

91. The '525 Patent specification states: "According to the principles of the present invention, there are alternate ways of storing and retrieving graphics and video data from unified frame buffer 107. For example, CPU 103 may write a static graphics background into part of the on-screen memory with the remaining "window" in the on-screen memory area filled with playback video data." CX 1, Column 6, lines 29-36.

92. The '525 Patent specification states: "It should be noted at this point that frame buffer 107 includes at least two different data areas or spaces to which data can be directed by the given address (either CPU 103 or controls 213 generated))]. Each space can simultaneously store graphics or video data depending on the selected display configuration." CX 1, Column 6, lines 13-18.

93. The terms "on-screen" and "off-screen" are described in the '525 patent as follows: "It should be noted at this point that frame buffer 107 includes at least two different data areas or spaces to which data can be directed by the given address ... Each space can simultaneously store graphics or video data depending on the selected display configuration. The on-screen area corresponds to the display screen; each pixel rastered out of a given pixel location in the on-screen area defines a corresponding screen pixel. The off-screen area is used to store data defining a window for selectively overlaying the data from the on-screen memory, fonts and other data necessary by controller 105." CX 1, Column 6, lines 13-25.

94. The Summary of the Invention" section of the '525 Patent includes the statement:

> The principles of the present invention in general provide for the flexible control of graphics and video data in a display control environment. In particular, an entire frame of video data, graphics

> data, or a combination of both, may be stored in on-screen memory and rastered out with the generation of the corresponding display screen. A window of graphics or video data can then be stored in off-screen memory and retrieved when the raster scan generating the display reaches the desired position on the display for the video window.

CX 1, Column 2, lines 41-50.

95. In opining on the "multi-format frame buffer" that Cirrus contends shares the same meaning as the "frame buffer", Mr. Ferraro stated "I also understand that graphics data can reside in either on-screen or off-screen memory and video data can reside in either on-screen or off-screen memory." CX 745C at 77 (Ferraro Rebuttal Report).

96. Claim 1 of the '525 Patent contains a reference to a "frame buffer" having on-screen and off-screen memory areas. CX 1, Column 14, lines 11-12.

97. Claim 13 of the '525 Patent contains references to a "frame buffer" having on-screen and off-screen memory areas. CX 1, Column 15, lines 31-32.

98. Claim 23 of the '525 Patent contains references to a "frame buffer". CX 1, Column 17, lines 18 and 22.

99. Claim 25 of the '525 Patent contains references to a "multi-format frame buffer" having on-screen and off-screen memory areas "each operable to simultaneously store data in graphics and video formats." CX 1, Column 17, lines 34-36.

100. Claim 37 of the '525 Patent contains a reference to a "multi-format frame buffer for simultaneously s[t]oring graphics and video data." CX 1, Column 18, lines 66-67.

101. Claim 40 of the '525 Patent teaches:

> The controller of claim 37 wherein said frame buffer is partitioned into on-screen and off-screen areas, each of said on-screen and off-

screen areas operable to simultaneously store both graphics and video data.

CX 1, Column 19, lines 12-15.

102. Claim 43 of the '525 Patent contains a reference to a "multi-format frame buffer having on-screen and off-screen areas each for simultaneously storing both graphics and video pixel data ...." CX 1, Column 19, lines 27-29.

103. On May 2, 1995, the '525 Patent applicants filed a first Information Disclosure Statement ("IDS") identifying eight prior art patents. In those remarks, the applicants indicated that the claims were allowable over the prior art references because the references did not "disclose or suggest a multi-format frame buffer in which both RGB and YUV data can be simultaneously stored in their original formats" and "neither of the Roskowski et al. references discloses dual backend pipelines for respectively processing graphics and video data retrieved from the frame buffer." CX 2 at 143-47.

104. The '525 Patent specification states that "Circuitry 200, 201, 202, 207, 208 is provided for writing a word of the pixel data received from the interface 206 to a one of the on- and off-screen memory areas corresponding to the address associated with the received word." CX 1, Column 3, lines 4-6.

105. Dr. Peuto testified that "writing selectively" involves writing data to the on-screen or off-screen memory spaces and means that "as I am writing to the on-screen and off-screen, I will do it selectively, probably based either on the fact it's on-screen, off-screen, or it's graphics or video." Peuto, Tr. at 1343.

106. Mr. Ferraro testified that "writing selectively" means that "this device can write each

word individually into either one of those spaces [on-screen or off-screen] of a frame buffer." Ferraro, Tr. at 489.

107. Mr. Ferraro testified: "The CPU can write a word of data that is going to be directed to the on-screen buffer, a piece of graphics data, and in the next cycle of time, choose to write a piece of video data which is going to written to the video region of the off-screen buffer. That is, to me, what I interpret selectively to mean." Ferraro, Tr. at 517.

108. Figure 2 of the '525 specification shows a CPU Interface 206. CX 1, Fig. 2.

109. The '525 Patent specification states:

> In the preferred embodiment of system 100, CPU 101 can write video data and/or read and write graphics data to frame buffer 107 via CPU interface 206. In particular, CPU 101 can direct each pixel to the frame buffer using one of two maps depending on whether that pixel is a video pixel or a graphics pixel. In the preferred embodiment, each word of pixel data ("pixel") is associated with one of two addresses, one which directs interpolation [sic] of the pixel as a video pixel through video front-end pipeline 200 and the other which direct interpolation [sic] of the pixel as a graphics pixel through write buffer 207 and graphics controller 208. As a consequence, either video or graphics pixel data can then be input to CPU interface 206 from the PCI/VI [sic] bus through a single "dual aperture" port as a function of the selected address.

CX 1, Column 5, lines 52-65.

110. Mr. Schafer testified as follows:

> Q Now, when you and I spoke at your deposition, you told me that the limitation in question, this first port limitation referred to the CPU interface 206; isn't that right? And that's in figure 2.
> A What's the reference again, please?
> Q It's 206 in the bottom left-hand portion of figure 2.
> A Okay, the CPU interface.
> Q And then you told me that this first port limitation relates to the host interface 206 receiving a word of data, decoding its address, and passing it to the

front end pipelines for processing; isn't that true?

A Yes.

Q And that's all you told me, correct? You didn't tell me anything about back end processing?

A Not that I recall.

Q And I didn't believe you. I sat there and argued with you for a good 10 minutes about this, didn't I?

A I don't remember.

Q I kept pressing you for how this host interface 206 directs the system to process the data in the back-end pipelines, and you kept telling me that was not the way it worked; isn't that true?

A Again, I don't recall the exchange.

Q Well, let me see if I can refresh your recollection a bit. If you turn to your deposition of November 6 at page 204, beginning at line 7. The question begins --

A The page again, please?

Q Page 204.

A Okay, I found it.

Q The question: "'A word of said data received with an address of said memory spaces directing said word to be processed as a word of video data or a word of graphics data,' can you give us your understanding of this phrase?

"Answer: That's referring to the dual aperture mapping which would direct the data through the graphics path that I defined a few minutes ago or the video path.

"Question: This is the same aperture mapping you described with respect to claim 12?

"Answer: That's my understanding.

"Question: And there is this phrase here that says 'directing said word to be processed as a word of video data or a word of graphics data.' Can you tell us your understanding of that directing phrase?

"Answer: Before the data is written to the frame buffer, it goes through an operation of graphics processing or operation of video processing. So referring to diagram 82, we're directing from the CPU interface 206 to either the graphics pipeline which or the input graphics pipeline which would be 235 or the video which would be 216. There is an address decoding and then a directing of the data to the appropriate processing block.

"Question: When you say there is an address

decoding, where does the address decoding take place in the '525 patent?

"Answer: In the CPU interface 206."

Was anything I read inconsistent with our front-end processing construction of claim 13?

A No.

Q Later, because I didn't believe you, I have to admit, I kept pressing. Later we came back to this, and I asked you whether you were sure that this did not relate to back end processing. At page 206, beginning at line 20, "question: Well, you said that the CPU interprets data as either graphics or video-based on its aperture address?

"Answer: Yes.

"Question: And then the data is placed in the frame buffer; correct?

"Answer: Correct.

"And then that data is retrieved from the frame buffer; correct?

"Answer: Correct.

"Question: And the data is forwarded to either the video or graphics pipeline; correct?

"Answer: I think we're getting beyond the scope of this.

"Question: Well --

"Answer: I'm not sure how that ties into answering the question.

"Question: Well, if you could just bear with me a little while, maybe we'll get through it. Do you remember the last question? The data retrieved from the memory buffer is directed into either the video or graphics pipelines; correct?

"Answer: That wasn't your last question. I thought your question was from the CPU interface, how the data is directed into either video or graphics, and you're talking about front-end processing. You've switched over to back-end processing.

"Question: Oh, I see. So you're interpreting the first port limitation here as a strictly front-end operation?

"Answer: Yes.

"Question: So the processing as a word of video data or a word of graphics data, you would describe to be so-called front end pipelines of the '525 patent?

"Answer: Yes."

Again, Mr. Schafer, you were educating me that this first port limitation is only, only directed to front-end processing; isn't that true?

A That appears to be the case.

Q And you made a point of making sure I understood that there was a mechanism within the first port for decoding the address associated with a particular word of data and directing it into either the front-end video or front end graphics pipelines; correct?

A Correct.

Q And you differentiated this mechanism from the dual aperture port saying that it could be something that forwards data to either the front-end video or graphics pipeline but did not have to be the dual aperture port; isn't that right?

A That's right.

Q And your interpretation of the first port limitation of claim 13 is that it includes any mechanism for taking an address associated with a data word and using that address to direct the data into either the front-end video pipeline or the front end graphics pipeline; correct?

A As we've just discussed, yes.

Schafer, Tr. at 660-64.

111. Mr. Ferraro testified that the "first port" limitation refers to the host port or PCI port, through which the CPU sends video and graphics data accompanied by addresses. Ferraro, Tr. at 489.

112. The term "frontend" is used to describe an element of a video graphics display controller which sits between the frame buffer and the host processor. Nally, Tr. at 134.

113. The term "backend" is used to describe an element of a video graphics display controller which sits between the frame buffer and the monitor. Nally, Tr. at 134; Ferraro, Tr. at 494.

114. Cirrus' Pre-Hearing Brief stated that the "first port" limitation of Claim 13 "... requires a

port through which data is received with addresses that tell the claimed device whether the data is video or graphics so that it will be properly processed." Cirrus Pre-Hearing Brief at 25

115. In diagrams he prepared in connection with his review of the '525 Patent, Mr. Ferraro represented the "first port" by noting "video or graphics?" next to an "address" identification. RX 504C at CL 120271; Ferraro, Tr. at 816-17.

116. The '525 Patent shows a VPORT interface 211 for receiving real-time video data. CX 1, Fig. 2.

117. The '525 Patent specification states: "Real-time video source 104 may be, for example, a CD ROM unit, a laser disk unit, a videotape unit, television cable outlet or other video data source outputting video data in a YUV format." CX 1, Column 5, lines 13-16.

118. Video is typically in YUV format. Ferraro, Tr. at 491.

119. Dr. Peuto stated that "video is now a term that is generally used to mean photorealistic real-time images encoded in YUV like television." ALJ 1 at 101.

120. The '525 Patent specification states: "Circuitry 201, 202 is provided for generating an address associated with a selected one of the memory spaces for each word of received real-time video data." CX 1, Column 3, lines 16-19.

121. The '525 Patent specification states: "In this instance, VGA controller 105 generates the required addresses into frame buffer 107." CX 1, Column 5, lines 11-13.

122. The '525 Patent specification states: "Data which is input through the video port 211 [is] address-free. In this case, video window controls 213 generates the required addresses to either the on-screen memory area or the off-screen memory as a function of display

location for the video window." CX 1, Column 5, line 66 - Column 6, line 3

123. Data received through the second port does not come in with addresses and, therefore, it is necessary to generate addresses for the incoming data so that it can be placed in the frame buffer. Ferraro, Tr. at 491.

124. The '525 Patent specification states: "Circuitry is also provided for selectively retrieving the words of data from the on-screen and off-screen spaces as data is rastered for driving a display." CX 1, Column 3, lines 21-23.

125. Mr. Ferraro testified, without offering support for this opinion, that "circuitry for selectively retrieving" means that each word can be selectively retrieved so that you are not forced to retrieve word 3 after word 2, but you would have the option, for example, of retrieving word 1 followed by 100. Ferraro, Tr. at 492.

126. Mr. Schafer affirmed his deposition testimony that:

> 'Selectively retrieving refers to the retrieval of graphics data within a graphics region, and the retrieval of video data within a video region of the display, and it doesn't necessarily mean at any point in time because the -- obviously, you have to grab the data ahead of time to display it. So there is some prefetching involved there. The selection is based upon the existence of a video window or existence of a graphics display and its position.'

Schafer, Tr. at 666.

127. At the end of each scan line, the scanning beam returns to the start of the next line. The periods of time during which the beam returns to the next line are called the "retrace" periods. ALJ 1 at 12-13.

128. Mr. Ferraro also described the definition of "rastered" as follows:

> Now, rastered, the viewable area on the screen is called the raster. The area of the screen in which data is displayed is called the raster. People refer to rastering the display as the providing of data to the display. Rastering also has a connotation of a two-dimensional. one-dimensional to a two-dimensional transformation so that we have a wire providing data to the monitor. That's one-dimensional. and that data is then parsed onto the screen in a two-dimensional fashion. You might use the term a typewriter rasters type onto a page, left to right, top to down format. "As data is rastered for driving a display" is a very important limitation in my mind.

Ferraro, Tr. at 492

129. Mr. Ferraro opined that:

> Rastering is the retrieval, processing, and providing of data from a frame buffer memory to a CRT/LCD display for the purpose of displaying pixel data .... The screen is refreshed by scanning a beam across the two-dimensional surface in a left-to-right and top-to-bottom sequence across the screen .... This process of providing data in a two-dimensional fashion is called rastering. In its most common usage, rastering implies the production of two-dimensional data to a CRT as retrieved from frame buffer memory.

CX 745C at 9 (Ferraro Expert Report).

130. Regarding the definition of "rastered" in the "circuitry for selectively retrieving" limitation of Claim 13, Mr. Ferraro testified as follows:

> A I think that the rastering there is referring to the providing of data to the display.
> Q In your expert report, you write -- and this is at page 9 of the report, which is under tab 3, "rastering is the retrieval processing and providing of data from the frame buffer memory to a CRT LCD display for the purpose of displaying pixel data." Is that consistent with your definition here in claim 13?
> A Yes. As I said when we first started the questioning regarding rastering, that I felt that it was a -- it was used as a metaphor, that it meant different things in different places, but the process of retrieving

data to put it on the screen is, in the largest sense, in my mind, rastering than the actual providing of the data onto the screen, that's also using the term rastering. And rastering out of memory is the more directed towards the memory, retrieving data out of memory. So I think it can be all three of those. I think it's used in all three.

Q So rastering is more than any one discrete element, it is a process; correct?

A No, that's not what I meant to say. What I meant to say is, in the one usage of the term, it's a process from start to finish. In another usage of the term, it relates to the retrieving of data out of memory. And in another usage of the term, it relates to putting data onto the screen, but it's -- the term "rastering" is used because it's that two-dimensional to one-dimensional transformation, or one-dimensional to two-dimensional.

Q The question is in the context of as data is rastered for driving a display, is rastered there a process or a discreet operation?

A I think there it's a bit of both. I don't think either conflict. I think you could read that to say as data is rastered for driving a display. Since you're already retrieving that data, that would indicate, okay, you're retrieving the data for the process of rastering to the display, and then it could also be read more tightly to say you're selectively retrieving the data as the data is being rastered onto the display. So I think that you could interpret it -- I think that you could interpret rastered in either of those contexts.

Q So it could mean both the discreet -- well, so it means, in your opinion, in this context, it means both a discreet [sic] operation of sending the data to the display as well as the process for getting it there?

A Yeah, I think it could be either one.

Ferraro, Tr. at 1654-55.

131. Mr. Ferraro explained the display raster as follows:

So what we saw is the dot going across the screen in sort of a typewriter fashion, one dot being displayed at a time, and this is referred to as "refreshing" a line. So a line of data is refreshed. Now, after the line of data is refreshed, just like our antique typewriters, it has to get back to the previous line. We do a carriage

return feed so it zips and comes back, ready to type the next line or display the next dot. This is called retracing or blanking, because no data is actually displayed in this time. It's just meant to get this scanning device back to the start of the next line ready for the next peice [sic] of data ... Afterwards, we have a retrace period where the beam is going down to the next line. This entire period of time represents the refreshing of one line, including the time to get back and ready for the next line.

ALJ 1 at 12.

132. Dr. Peuto refers to the active raster scan as the "active display period." Peuto, Tr. 1380

133. Mr. Ferraro also testified that in some contexts, "rastering" refers to a process of providing data to the display including the processing of data in the pipeline. Ferraro, Tr. at 1651.

134. Mr. Nally testified that "rastering" is taking data from the memory and sending it to the display device. Nally, Tr. at 174-75.

135. Mr. Nally's testimony supports an understanding of "raster" to include the entire process of retrieving and displaying data, with the entire display process, not just the active raster scan included. Nally, Tr. at 174-75.

136. The '525 Patent specification states:

In the preferred embodiment, data is continuously pipelined from on-screen memory through graphics back-end pipeline 205 to the inputs of output multiplexer 231. Window data from off-screen memory however is only retrieved from memory and pipelined through video backend pipeline 204 when a window is being displayed. In other words, when a window has been reached, as determined by control bits set by CPU 101 in VW control registers 222, video window display controls 222 generate addresses to retrieve the corresponding data from the off-screen memory space of frame buffer 107. Preferably, video FIFOs 223 and 224 are filled before the raster scan actually reaches the display window such that the initial pixel data is available immediately once the window has been reached. In order to insure that graphics memory data continues to be provided to graphics back-end pipeline 205, video window display controls 222 "steal" page cycles between page accesses to the graphics memory. It should be noted that

once the window has been reached the frequency of cycles used to retrieve window data increases over the number used to fill the video FIFOs when outside a window. When the frequency of window page accesses increases, video window display controls 222 arbiter 221 preferably "steal" cycles from page cycles being used to write data into the frame buffer.

CX 1, Column 9, lines 43-57.

137. A "pipeline" refers to a sequence of processing stages where the output of one becomes the input of another, and so on, in "assembly line" fashion. CX 745C at 12 (Ferraro Report). ALJ 1 at 83-84.

138. The '525 Patent specification states: "A first pipeline 205 is provided for processing data received from the on-screen area of frame buffer 107." CX 1, Abstract, lines 11-13.

139. The '525 Patent specification states: "A graphics backend pipeline processes ones of the graphics words of data retrieved from the frame buffer." CX 1, Column 3, lines 24-25.

140. Figure 2 of the '525 Patent shows the elements of backend graphics pipeline 205. None of the circuitry of the backend graphics pipeline is shared with the video pipeline 204. CX 1, Figure 2.

141. The "first pipeline" disclosed by Claim 37 processes for display graphics data retrieved from the frame buffer, and is therefore a backend pipeline. See CX 1, Column 19, lines

142. Mr. Ferraro testified that the video and graphics backend pipelines represent distinct and separate paths for the video and graphics data. Ferraro, Tr. at 500.

143. The '525 Patent specification states: "A second pipeline 204 is provided for processing data retrieved from the off-screen area of the frame buffer." CX 1, Abstract, lines 13-15.

144. In the first IDS to the Patent Office in connection with the '525 Patent application, prior art was distinguished from the '525 Patent invention based on the prior art not disclosing

"a pair of output pipelines for separately processing graphics (RGB) and video (YUV) data retrieved from the single frame buffer." CX 2 at 144.

145. The figures in the '525 Patent do not indicate that the graphics backend pipeline shares circuitry or elements with the video backend pipeline. CX 1.

146. The '525 Patent never makes reference to or suggests shared circuitry or elements between the graphics backend pipeline and the video backend pipeline. CX 1.

147. No party offered evidence that one skilled in the art would understand that two distinctly identified pipelines with different functions could share circuitry or elements.

148. The '525 Patent specification states: "... CRT controller 220, through arbiter 218 and memory interface 219, maintains a constant stream of graphics data into graphics backend pipeline 205 from memory; video or playback graphics data is rastered out only when a window has been reached by the display raster as determined by display position controls of window controls 222 (see FIGS. 3 and 5 and accompanying text) and CRT controller 220." CX 1, Column 8, lines 23-29.

149. The '525 Patent specification states: "... the static graphics are rastered out of the on-screen memory without interruption and passed through the graphics backend pipeline 205. The window of data in off-screen memory is rastered out only when the display position for the window has been reached by the display raster and is passed through video backend pipeline 204." CX 1, Column 6, lines 55-61.

150. Mr. Ferraro testified that this "always rastering" claim element means "that it's necessary to always retrieve the graphics data, so that even in those pixels that you're going to display video data, you still need to retrieve graphics data." Ferraro, Tr. at 495.

151. The '525 Patent specification states: "In order to insure that graphics memory data continues to be provided to graphics back-end pipeline 205, video window display controls 222 'steal' page cycles between page accesses to the graphics memory. It should be noted that once the window has been reached the frequency of cycles used to retrieve window data increases over the number used to fill the video FIFOs when outside a window. When the frequency of window page accesses increases, video window display controls 222/arbiter 221 preferably 'steal' cycles from page cycle being used to write data into the frame buffer." CX 1, Column 9, lines 57-67.

152. The '525 Patent specification states: "A video backend pipeline is provided for processing ones of the video words of data retrieved from the frame buffer, the circuitry for retrieving always rastering a stream of graphics data from the frame buffer to the graphics pipeline and rastering video data to the video backend pipeline when a display raster scan reaches a display position of a video window." CX 1, Column 3, lines 25-32.

153. The '525 Patent specification states: "Memory control circuitry 201 includes an arbiter 218 and a memory interface 219. Arbiter 218 prioritizes requests for access to frame buffer 107 received from video front-end pipeline 200, graphics controller 208 and bit block transfer circuitry 209. Arbiter 218 further sequences each of these requests with the refresh of the display screen of display 106 under the control of CRT controller 202." CX 1, Column 8, lines 7-14.

154. Mr. Bicevskis gave the following testimony:

> Q Now, there's actually an arbiter in the memory controller of the Rage Pro that prioritizes requests; correct?

A That's correct.

Q And the arbiter needs to do that because the memory controller gets requests for data or requests for -- access to memory, to be more precise, get requests for access to memory from a variety of functional blocks in the Rage Pro; correct?

A That is correct.

Q So it will get a request for a retrieval from, say, the graphics pipeline, and that might compete with a request for a retrieval from a video pipeline; correct?

A That is correct.

Q And indeed, it might compete with a request for a writing of data to memory from the memory controller; correct, not from the memory controller. Where does that request for writing come from?

A That would come from the host port.

Q So it has to --

A If it's host data coming in or it could come from a 2D entry or 3D entry.

Q So there are a variety of requesters for access to memory in the Rage Pro?

A That is correct.

Q So sometimes some of those requesters have to wait while the arbiter decides to give priority to another requester; is that correct?

A That's correct.

Q And that results in delays in the retrieval of data, delays as perceived, if you will, by the requester?

A That is correct.

Q And this is true for the Rage LT Pro and the Rage 128; correct?

A As well as any controller that uses DRAM.

Q Because this is a generic memory controller; right?

A Also by the nature of DRAM, you have to do things like refresh cycles, which means that you will, by definition of the device, stall the retrieval times.

Q So it's essentially inherent in the current design of display controllers that there will be -- that there needs to be the functionality of allocating access to memory in some sort of prioritized fashion among the various requesters?

A That is an accurate statement.

Q And indeed, it is virtually inherent in the design of a modern display controller that is perceived by any one of those requesters, there may well be delays in the access to memory that it has requested?

A That is correct.

Bicevskis, Tr. at 299-301.

155. The '525 Patent specification states: "Preferably, video FIFOs 223 and 224 are filled before the raster scan actually reaches the display window such that the initial pixel data is available immediately once the window has been reached." This refers to "prefetching" CX 1, Column 9, lines 54-57.

156. When "rastering" is used in connection with a memory retrieval operation, it includes prefetching. See CX 1, Column 6, lines 25-26 ("... both graphics and video data may be rastered *from the frame buffer* ...").

157. According to Mr. Ferraro, in the '525 Patent, video data only has to be retrieved when it is required to refresh the video portion of the window. Ferraro, Tr. at 537.

158. According to Mr. Ferraro, it makes no engineering sense to interpret "when" to mean "at the exact instant." A number of circuit elements sit between the monitor and the frame buffer. "All circuitry elements are going to impose a delay." Ferraro, Tr. at 538.

159. Delays inherent in rastering video data to the video backend pipeline include clocking delays, gate delays, arbiter imposed delays on the access to the frame buffer, and processing delays in the video backend pipeline. Ferraro, Tr. at 538-40.

160. It would be impossible for an engineer to "design a system that had no delay such that data can be retrieved instantly at the moment the CRT is at a particular point. . . There is no engineer that would be able to do that. It's not physically possible." Ferraro, Tr. at

545.

161. Mr. Ferraro stated that he does not "understand the meaning of when in this claim to be the exact same instant. When, in the context of this particular circuitry, means at the same time, given the necessary throughput delays of the related circuitry." Ferraro, Tr at 552

162. Mr. Ferraro identified Column 9, lines 54 through 60 of the '525 Patent as supporting an interpretation of "when" that allows for timing delays. CX 745 C at 62 (Ferraro Rebuttal Report).

163. Mr. Ferraro's preferred interpretation of "when" is that it means "in response to," in other words as data is needed for the video window. Ferraro, Tr. at 1647.

164. Mr. Schafer testified that "[o]bviously you have to grab the [video] data ahead of time to display it. So there is some pre-fetching involved there." Schafer, Tr. at 666. Mr. Schafer further testified that video "data must be fetched ahead of time or it could not keep up with the display. So the actual existence of [a] video window does have a bearing on when data is fetched, but it's not fetched at the precise moment that a pixel is to be output for display on the monitor." Schafer, Tr. at 667.

165. Mr. Bicevskis testified as follows:

> Q Now, Mr. Bicevskis, it would be quite hard to design a system that retrieved from memory -- let me set it up a little bit more clearly. We've got an arbiter. It's dealing with requests from various circuitry elements. We're back in January 1995. Then we've got FIFOs and we've got -- in the video pipeline.
>
> So we have the video pipeline stages that you and I discussed in your first testimony. And the arbiter as we discussed is a little unpredictable sometimes in figuring

out -- in determining when the video information is going to be displayed.

So with that set of assumptions, Mr. Bicevskis, isn't it true that it would have been very difficult -- I'm not going to say impossible, because who knows what's impossible. I'll be more of an engineer with you, very difficult to design a system in which circuitry for retrieving video data, sent it to the video pipeline at the same time a raster scan reached a video window display position on the screen?

A That's correct.

Bicevskis, Tr. at 1255-56.

166. Mr. Bicevskis agreed that it would be very difficult to design circuitry that could retrieve video data, send it to the video pipeline at the same time a raster scan reached a video window position on the screen. Bicevskis, Tr. at 1256.

167. Mr. Bicevskis agreed that several circuit elements related to the retrieval of data from memory impose delays on the data retrieval. Bicevskis, Tr. at 299-301.

168. Mr. Bicevskis' "hallway analogy" testimony regarding the feasibility of a system where video data is retrieved at the exact instant that the display raster scan reaches the display position of a window necessarily requires that "rastering" in the context of the "when" limitation not include pre-fetching. Bicevskis, Tr. at 1265-67.

169. "Rastering" in the context of the "when" limitation includes pre-fetching. See CX 1, Column 15, line 52 ("... rastering a stream of data *from said frame buffer* ..." (emphasis added)).

170. Mr. Ferraro testified as follows:

Q Let me ask it this way. Yesterday, you described the "when" condition as allowing for a certain amount of delay between the occurrence of the condition and the

retrieval of data from the frame buffer; isn't that true?

A Yes.

Q And so under your rubric, under your analysis, the condition you specified was, at a time prior to the display raster scan reaching the display window, the result being that you take data out of the frame buffer and pass it through the video pipeline; correct?

A Given the delays in the system, that was one of two possible meanings that I agree with.

Q I just want to make sure that the result is not in dispute. It doesn't sound like it's in dispute. The thing that has to happen is we're taking data out of the frame buffer and passing it through the video pipeline; correct?

A The rastering of data to said video back-end pipeline has to occur, and that is correct. I don't like saying that it is a result because I don't want my words turned against me -- meaning that I agree to your condition, but not the result. Okay.

Q Sure. We're going to talk about the condition. Let's go ahead and do that. So now there are two possibilities for the condition that I think I heard you say yesterday. Now, there are two possibilities. The first is that this when condition means "at the time that." So when would be replaced with at the time that a display raster scan reaches a display position of a video window.

A Are you including delays in that?

Q No, I'm not.

A But that's not consistent with the specification language.

Q Perhaps, and again, you and I are going to talk a lot about that. I'm just trying to get down on the board the two possibilities that I believe you identified yesterday. One was that this happens at the time that the display raster scan reaches the video window, and the other was at a certain time prior to the time that the display raster scan reaches a video window.

A Because is the time -- are you saying at the exact instant of time?

Q Yes, this means at the exact instant. Condition 1 -- or interpretation 1 means at the exact instance.

A Can you write exact on there, please.

Q At the exact time. And 2 was the other possibility that you offered, which was, I believe, at a

time prior to the exact time.

A That would be fine, yes.

Q The exact time, so those are two possibilities?

A I would like you to please qualify "prior" in that it's not just any arbitrary time prior. It's time prior with respect to engineering practice and as specified in the '525 specification.

Q Okay. Well, let's talk about that. How long prior?

A That's design-specific.

Q You can't tell us how long prior; isn't that right?

A If I was to look at any particular design and then knowing as we all agree that the arbiter introduces unpredictable delays, also given the fact that we have a two-dimensional system and not a one-dimensional system so that you can't -- you can say okay, I want to delay a certain number of pixels to the left because we have pixels, but you can't say I would like to go three quarters of a line ahead. You have to go pixels and lines in increments of 1. So given that, given a design, an engineer of average skill in the art could determine what the delay would need to be as specified in the '525 specification.

Q Okay. Let's just use the patent. I'm looking at the video pipeline, which is element 204 in figure 2; isn't that right?

A Yes.

Q And FIFO A seems to be the first, and then we've got decoder 225, interpolator 226, interpolator 227, color space converter 228, and then pixel doubler 237. Is that the video pipeline shown here in figure 2 of the '525 patent?

A Is that the video pipeline that you believe to be there?

Q I'm asking you, is that it?

A Yes, that is what I believe to be there.

Q All right. So the question is, how long is the delay through this video pipeline?

A There's a lot of parameters that feed into that. I think that the one that -- as I said, there's implementation-specific things with, how many delay stages do you have in your DAC? As Mr. Bicevskis indicated, there's delay in your scaler. As I indicated, whether

you're zooming or diminuating determines how much there is in the scaler. The FIFO, depending on what's happening, the FIFO determines it and then most important -- not most important, but most unpredictably, the arbiter in the circuit retrieval search.

Ferraro, Tr. at 719-23.

171. Mr. Ferraro also testified as follows:

Q So as I count back from the left edge of the video window, I'm going backward in time; correct?
A Yes, sir.
Q Now, I'm going to start counting the pixels back, and I want you to tell me when it is that I am beyond the time prior to the exact time as you define the "when" in the condition we're discussing in claim 13.
A I think in order for me to do that, we're going to have to talk about specific implementation. Would you like me to interpret the '525 and, as an electrical engineer and designer, design a system and tell you how I would do it?
Q I want you to focus on the '525 patent, on the system disclosed in the '525 patent.
A I am, sir, focusing on the '525 patent and the '525 patent is an architectural patent. I can't answer that question any more than I can answer the question how many AND gates are there in the scaler. That's a detail which is implementation-specific.

Ferraro, Tr. at 725.

172. Dr. Peuto testified as follows:

Q Well, 10 [sic], what does when mean to you?
A At this point it is -- it is probably possible to design a product that will do this, but it's more interesting to read the specification itself to try to find some guidance about what is the meaning of the word "when."
Q And what did you find when you read the specification?
A I have an exhibit that I can use to illustrate that.
Q This now is Exhibit RDX-34; is that correct?

A Yes.

Q Please use that.

A This is an exhibit in which we have taken an element of the '525 drawings called figure 3, which I believe is in its entirety, and we have taken a part of what I believe is figure 3, which is a figure that describe the type of signals that are driving the multiplexer, and the type of signal that are driving the multiplexer in that figure, the multiplexer is multiplexer 231, and it has some input that are the graphics and some inputs that are the video pipeline.

And the port called A and B are what makes you that you select either A or B -- excuse me, either the video or the graphics to then go to the latch and the DAC. And the implication, as we said, is the monitor is after the DAC 210. So this drawing suggests that between the comparisons of the screen raster scan and the definition of the window extent of the video window, there is very few gate delays that takes place before this signal is provided first through this multiplexer 304 and then to the line B of multiplexer 231.

So the fact that we had very few gate delays would suggest that the interpretation for the word "when" would be when taking into account those claim delays. I want to explain what is the likely value of those claim delays. We are talking a few nanoseconds in the kind of technology we're talking about. A nanosecond is a billionth of a second. So it's a very small amount of time.

Very often in the discussion, we have used the word "pixel time." This is because it's also a simple unit to use. On a 1024 by 768 monitor refreshing 72 times per second, the time it takes to draw one pixel to the next is 12 nanosecond, 12-1/2 nanosecond. So when we talk few nanosecond, we are in essence talking about few pixel time worth of time.

So then I conclude when I take this figure and the text that goes with it that explain things in more details, when I take this constraint from the specification and import it into the meaning of the claim, I find that I should expect to really start doing the fetching few pixel times before, which is what I mean to indicate by drawing a red rectangular region, which is offset in time, time, you know, move from left to right, offset in time by few pixel,

and although I probably have two or three in my drawing.

Q Dr. Peuto, based on your reading of the '525 patent, when does the circuitry in that patent start to retrieve data from the memory that's going to be displayed on the screen?

A Few pixel times before it hits the window.

Q And how does that relate to the diagram that you have there in front of you to your right?

A It is the time that it takes from those comparison to be prop you will gated to the --

Q And how -- what's your understanding of how Cirrus interprets the when portion of this claim?

A My understanding is Mr. Ferraro has come with a position that would say few pixel times before, like the same position I'm taking.

Peuto, Tr. at 1350-53.

173. The instantaneous retrieval of video data for display upon the active raster scan reaching the video window constitutes an engineering impossibility. Schafer, Tr. at 666-67; Ferraro, Tr. at 538, 545; see also Bicevskis, Tr. at 1255-56, 1260-62.

174. Persons of ordinary skill in the art would understand that the retrieval of video data for display involves some inherent engineering delays, and may involve pre-fetching, such that some of the retrieval is done in advance of the display. Peuto, Tr. at 1351-53; Ferraro, Tr. at 538, 545, 552; Schafer, Tr. at 666-67.

175. Cirrus did not present testimony or evidence regarding the understanding of one of ordinary skill in the art as to the amount of time in advance that pre-fetching should or would occur, or the amount of time that should or would be taken in video retrieval by engineering delays.

176. Cirrus' expert, Mr. Ferraro, testified that the length of time for pre-fetching or other engineering delays associated with video retrieval could not be quantified based on the

'525 Patent, but was design-specific. Ferraro, Tr. at 725.

177. Cirrus argues that the "when" limitation must "tak[e] into account predictable *and unpredictable* delays in retrieving and processing data." Cirrus Post-Hearing Brief at 43 (emphasis added).

178. The '525 Patent specification states: "An output selector is included for selecting for output between words of data output from the graphics backend pipeline and words of data output from the video backend pipeline." CX 1, Column 3, lines 32-35.

179. The '525 Patent specification states: "[T]he inputs to output multiplexer 231 are ... 16 or 24-bit color data directly from graphics backend pipeline 205 serializer 236 and 24-bit color data from the color look-up table 234 ...Depending on the mode, color comparison circuitry 302 compares selected bits from the overlay color key register 303 with either the 8 bits indexing look-up table 234 in the color look-up table mode (pseudocolor mode) or the 16-bits (24-bits in the alternate embodiment) passed directly from serializer 236." CX 1, Column 10, lines 4-28.

2. Claim 15

180. Claim 15 of the '525 patent reads as follows:

15. The controller of claim 13 wherein said output selector is operable to:

in a first mode, pass only a word of data output from said graphics pipeline;

in a second mode, pass a word of data output from said video pipeline when said display raster scan has reached a display position corresponding to a window and a word of data from said graphics pipeline when said display raster scan is in any other display position;

in a third mode, pass a word of data output from said video pipeline when said display raster scan has reached a display position corresponding to a window and a corresponding word of data from said graphics pipeline matches a color key and a word of data from

said graphics pipeline when said display raster scan is in any other display position; and

in a fourth mode, pass a word of data from said video pipeline when said corresponding word of data from said graphics pipeline matches a color key and a word of data from said graphics pipeline when said display raster scan is in any other display position.

CX 1.

181. Claim 15 depends on Claim 13. CX 1.

182. No dispute exists among the parties as to the proper construction of the "first mode" limitation of Claim 15.

183. The '525 Patent specification contains a description of the output selector circuitry. CX 1. Column 10, lines 1-14; Column 11, line 61 - Column 12, line 35. Claim 15 itself contains no such description of the output selector circuitry. CX 1.

184. According to Mr. Ferraro, the first mode means that the whole screen is being filled only with graphics data, and that only graphics data is passed. Ferraro, Tr. 557, 1602.

185. The '525 specification states: "In a second mode, a window of data is rastered from the off-screen memory when the display raster scan has reached the display window position and graphics data being rastered from the on-screen memory matches a color key." CX 1, Column 2, lines 55-59.

186. The "when" condition in the "second mode" limitation of Claim 15 refers to a different event than that referred to in the "when" limitation of Claim 13. With respect to the event referred to in Claim 15, the specification does not cite or describe any necessary delays or any pre-fetching of data. CX 1.

187. Mr. Ferraro testified as follows regarding Claim 15:

... In the second mode, pass a word of data output from said video

pipeline when said display raster scan has reached a display position corresponding to a window.

I want to break the claim element at that point. Our "when" word has popped up again. Now, here we're talking about when, but this time we're talking about -- if we're looking at it as a temporal relationship, we're not talking about a when which is going to pass data from the output of the video pipeline to the monitor.

Now, if we're talking temporally how much delay, there we can easily see it's going to be less delay than all the way back to the memory. So when, this use of the word "when" is consistent with both of my definitions, because it applies both to in response to, that the output selector has to passes the video data when the display, raster is at the video window in response to, and also when with the necessary delays.

Now, even at this far back end part of our device, still you can't read it instantaneously because there are still delays between the output selector and the final, just a lot less delay and perhaps more predictable delay than the full path of the data. And we continue 13B, and a word of data from said graphics pipeline when said display raster scan is in any other display position, so we've already described that case where we have a video window somewhere on the screen and all around it is the graphics data. The graphics data is going to be provided all around it, and the video data is going to be provided inside of it. So this mode precludes any graphics data from being displayed inside the video window. It's always video window inside, always graphics data outside.

Ferraro, Tr. at 557-58.

188. In practice, the "when" condition in the "second mode" limitation of Claim 15 does not by necessity involve the same degree of engineering delays or pre-fetching as are involved in the case of retrieving data in Claim 13, and in Claim 15's second mode, these delays are more predictable in nature. Ferraro, Tr. at 557-58. ATI offered no expert testimony to contradict Mr. Ferraro on this point.

189. According to Mr. Ferraro, the "second mode" limitation teaches the passing of video data in the video window, ignoring color keying. Ferraro, Tr. at 1603.

190. The '525 Patent specification states: "In a third mode, the window data is rastered out of the off-screen memory when the data being output from the on-screen memory matches the color key, notwithstanding the position of the raster scan." CX 1, Column 2, lines 59-62.

191. Mr. Ferraro testified that the "third mode" limitation allows for graphics data to be displayed inside the video window. This allows graphics data to occlude video data in the video window. Ferraro, Tr. at 560.

192. Mr. Ferraro testified that the "third mode" limitation teaches that both color keying and the window position have to be satisfied for the passage of data. Ferraro, Tr. at 1604.

193. Mr. Ferraro explained that color keying requires the selection of a particular color for use as the key. If the graphics data matches that color, then video is selected for display. ALJ 1 at 31-32.

194. Dr. Peuto explained color keying as "selecting two streams of data and you're making a choice based on a specific key, a specific color, a choice that was predetermined before . . . ." ALJ 1 at 87-88.

195. The '525 specification states: "[T]he inputs to output multiplexer 231 are ... 16 or 24-bit color data directly from graphics backend pipeline 205 serializer 236 and 24-bit color data from the color look-up table 234 ...Depending on the mode, color comparison circuitry 302 compares selected bits from the overlay color key register 303 with either the 8 bits indexing look-up table 234 in the color look-up table mode (pseudocolor mode)

or the 16-bits (24-bits in the alternate embodiment) passed directly from serializer 23c "

CX 1, Column 10, lines 4-28.

196. Dr. Peuto asserted "And a word is a collection of byte[s]." ALJ 1 at 102.

197. In the third mode of Claim 15, the data from the graphics pipeline that is compared against the color key value consists of a "word". CX 1, Column 16, lines 6-12, Column 10, lines 4-28.

198. According to Cirrus and Mr. Ferraro, the "fourth mode" limitation teaches that window position is to have no effect on the decision to pass video. Ferraro, Tr. at 1605.

199. Mr. Schafer testified as follows:

> Q Now we get to the fourth mode.
> A Within the video.
> Q Within the video window; correct?
> A That's right.
> Q Now we get to the fourth mode, and the fourth mode is kind of a mixed metaphor, isn't it?
> MR. JACOBS: Your Honor, I'm going to have to object on -- I know you had cautioned us, but a mixed metaphor question I just don't understand.
> JUDGE MORRISS: Could you rephrase it, please.
> BY MR. CORDELL:
> Q Well, Mr. Schafer, the fourth mode of claim 15 is unclear to you; isn't that right?
> A It's confusing.
> Q In fact, it is missing an essential statement about what to do when inside the video window; isn't that right?
> A It says "in any other display position" without stating the display position. So it's confusing.
>
> Schafer, Tr. at 623-24.

200. Dr. Peuto testified as follows:

> Q And then the fourth mode?

A I have to tell you I can't parse that fourth mode.
Q What's the word you were using?
A I cannot parse it. I cannot understand it.
Q What's the difficulty you have with it?
A It's the issue of certainly saying "is in any other display position," and at this point I just do not know what this claim is meant, and your Honor, as you may know -- I just don't.

Peuto, Tr. at 1357.

201. Cirrus changed its position as to the proper construction of the "fourth mode" limitation between its post-hearing brief and its reply brief. Cirrus Post-Hearing Brief at 57; Cirrus Reply Brief at 30.

202. The reference to "when said display raster scan is in any other display position" in the "fourth mode" limitation is inconsistent with an exclusively color key system. In the context of a description of a color key system, the reference to "when said display raster scan is in any other display position" is nonsensical and unintelligible. See Peuto, Tr. at 1357; Schafer, Tr. at 623-24.

203. "[A]ny *other* display position", as set forth in the "fourth mode" limitation, lacks an antecedent reference. CX 1; Schafer, Tr. at 623-24..

3. Claim 16

204. Claim 16 of the '525 Patent reads as follows:

16. The controller of claim 13 wherein said video pipeline includes a first first-in-first-out memory for receiving a plurality of words of data for a first display line of pixels in memory and a second first-in-first-out memory or receiving a plurality of words of data from a second display line of pixels in memory.

CX 1.

205. Claim 16 depends on Claim 13. CX 1.

206. The '525 Patent specification does not define the meaning of a "first-in-first-out memory" CX 1

207. The term FIFO is well known to a person of ordinary skill in the industry as a memory structure in which data are written into the memory in the same order they are read out of the memory, hence the name first-in-first-out. Peuto, Tr. at 1360. RX-617C at 12. CX 745C at 13 (Ferraro Expert Report).

208. Neither of the FIFOs taught by Claim 16 operates as a write buffer, holding data destined for memory, as such a finding would be inconsistent with the description of the function of the FIFOs in the '525 Patent specification as receiving data for the generation of the on-screen display. CX 1, Column 8, lines 33-36, lines 44-51.

209. "Display line" is the pixel data that represents the information to be put on the monitor. Ferraro, Tr. at 688.

210. The phrase "display line of pixels in memory" refers to the pixel data that represents a horizontal display row on the monitor. Ferraro, Tr. at 688; see also ATI Post-Hearing Brief at 50.

4. Claim 17

211. Claim 17 of the '525 Patent reads as follows:

> 17. The controller of claim 16 wherein said first display line is stored adjacent in memory to said second display line.

CX 1.

212. Claim 17 depends on Claim 16. CX 1.

213. "Adjacent" means that in two-dimensional space adjacent lines are one directly above the

other. In one-dimensional space. the lines are horizontally neighboring. Ferraro. Tr at 68-

214. Mr. Schafer testified as follows:

> Q Claim 17 says that the first display line that stored adjacent in memory to the second display line. Can you give us your understanding of that phrase?
>
> A That the pixels in the first display line are stored sequentially from some address, and immediately after the last pixel in the first display line, the pixels from the second display line are stored sequentially from that address on.
>
> Q Now, turning back in the specification to column 8, line 40, it refers to a pair of lines as being N minus 1 and N plus 1 in memory. Do you see that?
>
> A Yes, I do.
>
> Q Does this mean that these two lines would, in fact, not be adjacent in memory?
>
> A I would say that this is talking about source lines N minus 1 and N plus 1 which would indicate to me there's a two line separation in memory, not adjacent.

Schafer, Tr. at 630.

215. Mr. Ferraro testified as follows:

> Q And with respect to -- can you comment on claim 17, please?
>
> A Claim 17 requests that the said first display line is stored adjacent in memory to said second display line. Now, in memory, we have this storage in the left to right contiguous memory of our lines of data. And this claim is stating that the first display line is stored adjacent in memory to the second display line, and in the specification, it describes adjacent display lines, and it also has in my opinion a typographical error, and it talks about two display lines being N minus 1 and N plus 1, and I have to confess it took me twice to realize that that is a mistake, that N minus 1 and N plus 1 are not adjacent and that really N minus 1 and N would be adjacent or N and N plus 1 would be adjacent. I think the use of the word adjacent is pretty

well known and that that can be written off as a typographical error.

Ferraro, Tr. at 687.

216. ATI points to no expert testimony by its technical experts regarding the meaning of the adjacent storage in Claim 17.

5. Claim 23

217. Claim 23 of the '525 Patent reads as follows:

23. The circuitry of claim 13 wherein said video pipeline comprises:

a first-in/first-out memory for receiving a first stream of words of data from said frame buffer;

second first-in/first-out memory disposed in parallel with said first first-in/first-out memory for receiving a second stream of words of data from said frame buffer; and

interpolation circuitry for selectively generating an additional word of data by interpolating a word of said first stream and a word of second stream data output from said first and second first-in/first-out memories.

CX 1.

218. Claim 23 depends on Claim 13. CX 1.

219. The '525 Patent specification states: "Backend video pipeline 204 further includes a Y interpolator 226 and X interpolator 227." CX 1, Column 8, lines 62-63.

220. The '525 Patent specification states: "An interpolator is provided as part of the video pipeline for generating additional data by interpolating data output from the first and second first-in/first-out memories." CX 1, Column 3, lines 64-67.

221. The '525 Patent specification states: "The output of X interpolator 227 is passed to a color converter 228 which converts the YCrCb data into RGB data for delivery to output

multiplexer 304." CX 1, Column 9, lines 8-10.

222. The '525 Patent specification states: "In the preferred embodiment, during Y zooming (expansion) Y interpolator 226 accepts two vertically adjacent 16-bit RGB or YCrCb pixels from the decoder 225 and calculates one or more resampled output pixels using a four subpixel granularity. X interpolator 227 during X zooming (expansion) accepts horizontally adjacent pixels from the Y interpolator 226 and calculates one or more resampled output pixels using a four subpixel granularity. For data expansion using line replication, Y interpolator 226 is bypassed. Y interpolator 226 and X interpolator 227 allow for the resizing of a video display window being generated from one to four times." CX 1, Column 8, line 62 - Column 9, line 7.

223. Interpolation differs from replication: in replication you simply copy each pixel, in interpolation you estimate new values of what should be in between two existing pixels. ALJ 1 at 36-37.

224. Dr. Peuto explained the difference between replication and interpolation: "The simplistic mechanism . . . deals with replicating the pixels and the more complex mechanism does some averaging operation on the pixels in order to be able to blow up the image and have less granularity." ALJ 1 at 92-93.

B. <u>Whether ATI's Rage Devices Infringe the Inserted Claims</u>

1. Claims 13 and 37

225. The ATI Rage Devices are video and graphics controllers. Bicevskis, Tr. at 266; Peuto, Tr. at 1339.

226. The ATI Rage Devices have a frame buffer divided into on-screen and off-screen

memory areas. Bicevskis, Tr. at 1112-13, 1120.

227. The ATI Rage Devices store [

] CFF 498; Bicevskis, Tr. at 1120

228. The ATI Rage Devices [

] Bicevskis, Tr. at 1120; Peuto, Tr. at 1534.

229. Mr. Ferraro testified that the ATI Rage Devices have circuitry for writing selectively words of received data into the on-screen or off-screen memory. Ferraro, Tr. at 508-09.

230. The ATI Rage devices have circuitry to selectively write graphics and video data into on-screen or off-screen memory according to the addresses accompanying the data. Bicevskis, Tr. at 277-78, 284-85.

231. The ATI Rage Devices have a bus interface [

] ATI Post-Hearing Brief at 30-31; RFF 271; Bicevskis, Tr. at 277-78, 284-86.

232. Mr. Bicevskis explained [

] Bicevskis, Tr. at 279, 283.

233. Dr. Peuto believes the ATI Rage Devices meet the "second port" limitation of Claim 13. Peuto, Tr. at 1345.

234. Mr. Ferraro testified that the ATI Rage Devices have a video port for receiving real-time video data. Ferraro, Tr. at 518-19.

235. The ATI Rage Devices have a video port for receiving real-time video data. Peuto, Tr. at 1345; Ferraro, Tr. at 518-19.

236. Mr. Bicevskis testified as follows:

[

]

Bicevskis, Tr. at 295-96.

237. Mr. Ferraro testified that [

] Ferraro, Tr. at 521.

238. The ATI Rage Devices contain circuitry for generating an address associated with a selected one of the memory areas for real-time video data received through the video port. Bicevskis, Tr. at 295-96; Ferraro, Tr. at 521.

239. Mr. Bicevskis testified as follows:

[

]

Bicevskis, Tr. at 296-99

240. Mr. Bicevskis testified [

] Bicevskis, Tr. at 301-02.

241. Mr. Bicevskis' testimony from transcript pages 296-302 indicates his inclusion of both graphics and video data in his description of the retrieval of "data". Bicevskis, Tr. at 296-302.

242. Mr. Bicevskis testified [

] Bicevskis, Tr. at 1200.

243. The ATI Rage Devices contain circuitry for selectively retrieving graphics and video data from on-screen and off-screen areas as data is rastered for driving a display. See Bicevskis, Tr. at 296-302; 1000-001.

244. The ATI Rage Devices have a graphics backend pipeline and a backend video pipeline. Bicevskis, Tr. at 303-04.

245. In testifying to the existence of the graphics backend pipeline and the video backend pipeline, Mr. Bicevskis never stated or suggested that they shared circuitry or elements. Bicevskis, Tr. at 303-04.

246. Dr. Peuto testified as follows:

[

]

Peuto, Tr. at 1341-42, 1347.

247. ATI offered no affirmative evidence that the ATI Rage Devices' graphics backend pipeline and video backend pipeline share circuitry or elements.

248. The graphics backend pipeline and the video backend pipeline in the ATI Rage Devices [

] See Bicevskis, Tr. at 303-04; Peuto, Tr. at 1341-42, 1347.

249. The ATI Rage Devices' retrieval from the frame buffer and sending of data to the graphics backend pipeline [

] Bicevskis, Tr. at 304, 307.

250. The ATI Rage Devices contain circuitry for retrieving always rastering a stream of data from the frame buffer to the graphics backend pipeline. See Bicevskis, Tr. at 304, 307.

251. The ATI Rage Devices retrieve video data [

] Peuto, Tr. at 1546-1547.

252. In light of its indefiniteness, the "when" limitation of Claim 13 cannot be applied to the ATI Rage Devices for purposes of an infringement analysis.

253. The ATI Rage Devices have output selector circuitry to select between data output from the graphics backend pipeline and data output from the video backend pipeline. Peuto, Tr. at 1354; Ferraro, Tr. at 556.

2. Claim 15

254. In light of its indefiniteness, Claim 15 cannot be applied to the ATI Rage Devices for purposes of an infringement analysis.

3. Claims 16, 17 and 23

255. The ATI Rage Devices contain [ ] See Hall, JX 8C at 89; Bicevskis, Tr. at 317, 324, 1147; Schafer, Tr. at 600-01, 624-26; Nally, Tr. at 157.

256. The ATI Rage Devices do not contain two FIFOs. Peuto, Tr. at 1358-60; Bicevskis, Tr. at 327-28, 1174.

257. A line buffer serves as a delay element that accepts and holds data. Ferraro, Tr. at 685-86.

258. In the ATI Rage Devices, [ ] Ferraro, Tr. at 685-86.

259. The line buffer(s) in the ATI Rage Devices perform the same function and achieve the same result as the dual FIFOs described in the '525 Patent. Ferraro, Tr. at 679-87.

260. Oswin Hall [

] Hall. JX 8C at 89-99.

261. Oswin Hall [

]

Hall, JX 8C at 91-92.

262. Mr. Ferraro offered credible expert testimony that, from the standpoint of one skilled in the art, the ATI Rage Devices' line buffer(s) constitutes an equivalent both to the first FIFO and to the second FIFO set forth in the '525 Patent. Ferraro, Tr. at 672-89.

263. Mr. Ferraro's testimony [

] Ferraro, Tr. at 672-89; Hall, JX 8C at 89-99.

264. Dr. Peuto testified as follows:

[

]

Peuto, Tr. at 1359-60 (emphasis added).

265. Dr. Peuto's testimony at Tr. 1359-60 regarding the ATI Rage Devices' line buffers is inconsistent with Mr. Hall's statements regarding the functionality of the ATI Rage Devices' line buffer(s). Peuto, Tr. at 1359-60; Hall, JX 8C at 89-99.

266. The ATI Rage Devices' line buffer(s) is equivalent to the dual FIFOs described in Claims 16, 17 and 23 of the '525 Patent.

III. Validity

A. On-Sale Bar

267. It is conclusively established for purposes of this investigation that Cirrus offered for sale CL-GD7542 Nordic product ("Nordic Product") in the United States before January 23, 1994. See Cirrus Notification (4/27/99).

268. Cirrus offered no direct evidence that the Nordic Product was *not* placed on sale in the U.S. before January 23, 1994.

269. Cirrus' Robert Dickinson testified as follows:

[

]

Dickinson, Tr. at 391.

270. Mr. Dickinson never directly testified that Cirrus made no offer to sell the Nordic Product prior to January 23, 1994. See Dickinson. Tr. at 336-429.

271. Cirrus identified [

]

272. In 1993, Cirrus [

]

273. [

]

274. [

]

275. [

]

276. [

]

277 [

]

278. [

]

279. [

]

280. No party offered direct evidence of actual sales of the Nordic Product prior to January 23, 1994.

281. [

]

282. [

]

283. [

]

284. [

]

285. The Nordic Product invention was ready for patenting as of January 23, 1994. See *supra*.

286. [

] [ ]

287. [

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288. [

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289. [

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290. [

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291. [

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292. [

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293. [

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294. [

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295. [

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296. [

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297. [

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298. [ ]

299. [

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300. [

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301. [

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302. [

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303. [

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304. [ ]

305. [

306. [

]

307. [ ]

308. As to Claim 37, Cirrus raises no technical arguments against the Nordic Product practicing this claim. Cirrus Post-Hearing Brief; Cirrus Reply Brief.

309. As to Claim 13, Cirrus limits its arguments against the Nordic Product practicing this claim to the video port/address generation circuitry and the "always rastering" limitations Cirrus Post-Hearing Brief; Cirrus Notification (4/27/99).

310. The indefiniteness of the "when" limitation of Claim 13 precludes application of that claim limitation to the Nordic Product.

311. [

]

312. [ ]

313. [

]

314. [

]

315. [

]

]

316. In the passage quoted above, [ ] seemed to misunderstand the questioning, to lack the necessary knowledge to respond, or to provide nonresponsive answers. [

]

317. The Nordic technical specification does not clearly and directly indicate whether the Nordic Product satisfied the "always rastering" limitation, and neither party offered adequate expert testimony to clarify the specification. See CX 102C.

318. When confronted on cross examination with certain statements from the Nordic 1M Specification and the Nordic Preliminary Data Book, Dr. Peuto was not able to explain why he concluded that the Nordic 7542 continued to retrieve graphics even when it was displaying video data. Peuto, Tr. at 1501-10.

319. Dr. Peuto testified that the CRT address counter relates to fetching graphics data into the graphics FIFO. Peuto, Tr. at 1502. Dr. Peuto further admitted that when video is displayed, the CRT address counter is stopped to avoid a wrong count, meaning that the retrieval of graphics data from memory and into the "incoming port" of the graphics FIFO is stopped. Peuto, Tr. at 1502-04. Dr. Peuto asserted that graphics data would continue to flow out of the graphics FIFO into the rest of the graphics pipeline, and that the graphics FIFO would need to be refilled once it was emptied. However, Dr. Peuto did not point to any specific evidence in the Nordic documentation to support this point, nor did he assert that graphics data would continue to be retrieved for each pixel location on

the screen. Peuto, Tr. at 1504.

320. ATI did not point to evidence as to the obviousness of combining the "always rastering" feature with the Nordic Product.

B. Section 102(b) – Anticipation

1. Oak/Brooktree

321. Oak/Brooktree refers to the combination of two products made by two different companies: the Oak Spitfire OTI-64107, and the Brooktree Bt885. Peuto, Tr. at 1364-68; see RX 239 (Brooktree Bt885 specification), RX 254 (Oak Spitfire specification).

322. Jonathan Siann was the architect for the Bt885. Siann, Tr. at 990-92.

323. Mr. Siann worked with Oak Technology to design the Oak Spitfire following the proposed architecture he designed for an interface with the Bt885. Siann, Tr. at 998.

324. The Oak Spitfire was designed to interface with the Bt885. Siann, Tr. at 1040; CX 745C at 58 (Ferraro Rebuttal Report).

325. The January 1994 Oak Spitfire specification contains a technical diagram showing both the Oak Spitfire product and the Bt885. See RX 254 at ATI 018065-66; Peuto, Tr. at 1364-68.

326. The Oak Spitfire and the Bt885 are separate chips. Peuto, Tr. at 1365.

327. The Bt885 was sold by the end of 1993. Siann, Tr. at 999.

328. The Oak Spitfire was sold prior to January 23, 1995. [

] Nguyen, JX 15C at 24.

329. An article published in the June 1993 edition of Electronic Design magazine referenced and discussed the Oak Spitfire product and the Bt885. Siann, Tr. at 999; RX 251C.

330. The Electronic Design article included a diagram similar to the drawing in Oak's Data Book (RX 250). Nguyen, JX 15C at 12.

331. ATI failed to point to any expert testimony from the perspective of one skilled in the art that the material in the June 1993 edition of Electronic Design includes an enabling description of the relevant architecture.

332. An article published in the July 5, 1993 edition of Electronic Engineering Times referenced and discussed the Oak Spitfire product and the Bt885. RX 252.

333. ATI failed to point to any expert testimony from the perspective of one skilled in the art that the material in the July 5, 1993 edition of Electronic Engineering Times includes an enabling description of the relevant architecture.

334. Mr. Siann gave a public slide presentation on the Bt885, with no nondisclosure agreement, at a conference in March 1993. Siann, Tr. at 994-95.

335. ATI failed to point to any expert testimony from the perspective of one skilled in the art that the material in Mr. Siann's slide presentation included an enabling description of the relevant architecture.

336. Mr. Nguyen, the Oak Spitfire project manager, testified that he could not recall whether [

]

Nguyen, JX 15C at 20-21, 23.

337. Mr. Nguyen testified that typically, engineering versions of specifications [

] Nguyen, JX 15C at 21.

338. ATI pointed no testimony other than Mr. Nguyen's regarding the public availability of the January 1994 Oak Spitfire specification [RX 254].

339. Mr. Nguyen testified that [

] Nguyen, JX 15C at 21.

340. Mr. Nguyen testified that he did not know [

] Nguyen, JX 15C at 21.

341. Regarding the invention date for the '525 Patent invention, Mr. Nally testified as follows:

> Q Let's see if we can get the chronology down. Do you recall when you were doing this thinking about a solution to the problem?
>
> A Yeah. It was over the summer of 1993.
>
> Q And what do you recall about the events of that summer in connection with this analysis? Do you recall some back-and-forth with management on your proposed solution?
>
> A Okay. I actually made -- during the summer, I was putting together my ideas. Either sometime late summer or early fall, I presented management with my first proposal, and they reviewed the proposal, and they actually rejected it. They said it was too risky. They thought it was overdone. And the reason why it was rejected is because I was at that point saying that we really need two video windows, not just one, but two video overlay windows.
>
> And the reason I was doing that, if you remember, I was working on the 2070 and 2080 and I still saw a great need for video conferencing. I was trying to bring not only multimedia to the PC but also teleconferencing capability to the PC. In order to bring teleconferencing to the PC, you needed two video overlay windows.
>
> So my proposal actually went further than what they asked for. They said give me just rudimentary video for windows playback mode, and I gave them something that was more than what they wanted. So they rejected it.

Q What happened next?

A I went back and redid my proposal. I toned it down. I reduced it down to one video window, left the video port in there, and resubmitted it.

Nally, Tr. at 66-67.

He subsequently testified that the second proposal was also rejected, and he continued his back-and forth with management. Nally, Tr. at 67-70.

342. Mr. Schafer testified as follows:

Q Mr. Schafer, I ask you to turn to tab 1 of your binder, which is a copy of the '525 patent, and I'd like to ask you, when did you begin working on the concepts that led to this patent?

A I began working on this in the summer of 1993 with Robert Nally and continued working on it through the fall of1993 and then into 1994.

Schafer, Tr. at 565-66.

343. Regarding work on the '525 Patent invention, Mr. Schafer testified as follows:

Q Let's turn to tab 2, which is CX-30. Can you tell us what this document represents?

A Yes. This was a architectural proposal generated by Robert Nally in the fall of 1993. It describes the state of our discussions at that time regarding this architecture.

Q Does this document reflect all the features that were finally implemented by you?

A No. It was the primary ideas, but we actually refined some of the sections over the course of the next couple of months, added more detail.

Q Let's turn to tab 3, which is CX-31, and can you tell us what the purpose of this document was?

A This is a later version of the document we just talked about distributed to more of the marketing and management team to indicate the current state of our progress on the architecture and to give a list of features and the current state and some detail on those features.

Q. Does this document reflect all of the details that you implemented?

A No. There were some pieces missing. Some of it is regarding the level of detail that we later developed. and some features were actually not included in the documentation that Robert was generating, primarily because they weren't approved -- in the approved features set from our management at the time. Robert and I had discussions on the insertion video port for capturing video. We had some of our own ideas we wanted implemented, but they weren't deemed important enough to delay the schedule for this product, so they were left out of the initial documentation.

Q Now, do you recall at the time that this document was generated whether you were actually working on those details that were left out?

A Yes. We had discussed the -- for instance, the video, we discussed that over the course of the summer because that was a feature we had in some of our existing products, not the video integrated, but stand-alone video. So the work was being done on this but not in this widely distributed documentation.

Q Was this the first proposal that Mr. Nally gave to management?

A I don't recall if this was the first or not. This was obviously not the first revision of this document, but I don't know if this is the first one that management saw.

Schafer, Tr. at 567-68.

344. The October 1993 and the November 1993 proposal documents by Mr. Nally, CX 30C and CX 31C, do not reflect the final structure of the '525 Patent invention; some features of the '525 Patent invention were not included on the documents. See CFF 238, 240, 244, 246, 247; Schafer, Tr. at 567-68.

345. See additional findings of fact regarding Oak/Brooktree, *infra*, under Section 102(a).

2. Intel i750

346. Dr. Lawrence Ryan was a co-architect of the Intel i750. Ryan, JX 23C at 16.

347. The Intel i750, manufactured by Intel Corporation, includes the 82750 Display Processor, the 82750 Pixel Processor and video digitizer circuitry. Peuto, Tr. at 1430-31; RX 492 at ATI 057155; RX 264 at ATI 019398.

348. The Intel i750 was on sale more than one year prior to the filing of the '525 Patent application, *i.e.* before January 23, 1994. Ryan, JX 23C at 13-18; RX 275C; RX 137; RX 276C.

349. The Intel i750 was in public use more than one year prior to the filing of the '525 patent application, i.e. before January 23, 1994. Ryan, JX 23C at 13-18; RX 275C; RX 137; RX 276C.

350. Both graphics and video data are stored in the frame buffer memory of the Intel i750 Ryan, JX 23C at 49, 75; Peuto, Tr. at 1324; Peuto Expert Report at 39 (RX 616C); Ferraro, Tr. at 1576-77.

351. The i750 frame buffer [

] Ryan, JX 23C at 50, 72-73; DB Guide at ATI019717, ATI019766 (RX 262C); RX 493C; RDX-23C.

352. The i750 memory has on-screen and off-screen areas. Ryan, JX 23C at 74-75; Peuto, Tr. at 1438-39; RX 493C; RDX-23C; Ferraro, Tr. at 1577.

353. In the i750, [

] Peuto, Tr. at 1438; RX 493C; RDX-23C.

354. In the i750, [

] Peuto, Tr. at 1438-1439; Ferraro, Tr. 1577; RX 493C; RDX-23C.

355. In the i750, [

] Peuto, Tr. at 1439; Ferraro, Tr. at 1577; RX 493C; RDX-23C

3. Parallax 1280/Viper

356. Parallax Graphics Inc. sold the Parallax 1280 product beginning in early 1984, and sold the VIPER product beginning in 1988 (both products collectively referred to as "Parallax 1280/Viper"). Order No. 38 at 8.

357. The Parallax 1280 and the VIPER products have essentially the same features and functionality. RX 615 at 13.

358. Mr. William Mears was the architect of the Parallax 1280/Viper. Mears, Tr. at 863.

359. The Parallax 1280/Viper could operate in two modes: [

] Mears, Tr. at 892, 932-33.

360. In the normal, [

] Mears, Tr. at 892.

361. Mr. Mears' testimony served as the primary, or at least essentially the sole comprehensive source of information on the [ ]

362. Mr. Mears testified as follows:

[

]

Mears, Tr. at 935-37.

363. Mr. Mears' testimony contained internal inconsistencies and/or lacked clarity on certain aspects of the [ ] mode of the Parallax 1280/Viper, which were not clarified by other evidence. See e.g. Mears, Tr. at 935-37.

C. **Section 102(a) - Known by Others**

364. The Oak Spitfire and the Bt885 were sold to the public prior to January 23, 1995. Nguyen, Tr. at 16-17; Siann, Tr. at 999.

365. The Oak Spitfire specification dated [

] Nguyen, Tr. at 15-16.

366. The Oak Spitfire specification indicates that the frame buffer has "two different places", a "graphics data area" and a "video data area". RX 254 at ATI 018061.

367. Mr. Siann explained that in interfacing the Bt885 and the Oak Spitfire, the on-screen region of the frame buffer corresponds to graphics data, and the off-screen area corresponds to video data. Siann, Tr. at 1068.

368. In explaining his slide presentation on implementing the Bt885 with a product such as the Oak Spitfire, which had a single frame buffer, Mr. Siann stated that "...the biggest block in the frame buffer will be the on-screen graphics memory ...." Siann, Tr. at 1009-10.

369. In explaining his slide presentation on implementing the Bt885 with a product such as the Oak Spitfire, which had a single frame buffer, Mr. Siann testified that the off-screen memory would typically store video but could also store other "things like fonts or cursors or more graphics." Siann, Tr. at 1012.

370. Mr. Siann's testimony indicates that when used in connection with the Bt885, video was only stored off-screen area of the Oak Spitfire frame buffer. See Siann, Tr. at 1009-10. 1068. Mr. Nguyen testified that [

] Nguyen, JX 15C at 40.

D. Section 102(e) - Patented by Others

1. The Siann '306 Patent

371. U.S. Patent No. 5,406,306 ("Siann '306 Patent") issued on April 11, 1995, and was based on an application filed on February 5, 1993. RX 4.

372. The Siann '306 Patent is related to the Brooktree Bt885. Peuto, Tr. at 1369; CFF 951.

373. The '525 Patent applicants disclosed the Siann '306 Patent to the patent examiner during prosecution. CX 2 at 161-63.

374. ATI's expert, Dr. Peuto, was previously retained in connection with a lawsuit between Brooktree and S3 involving the Siann '306 patent. Dr. Peuto worked together with Dr. Ryan of Intel on that case. Peuto, Tr. at 1370-71.

375. In connection with the Brooktree/S3 litigation, Dr. Peuto worked together with Dr. Ryan on claim charts regarding the Siann '306 patent that were attached to a declaration that Dr. Ryan submitted in that litigation. In particular, Dr. Peuto worked on the "clarified function" and "structural notes" columns of those claim charts. Peuto, Tr. at 1371-76.

376. In preparing his expert report on the '525 patent, Dr. Peuto relied on Dr Ryan's declaration regarding the Siann '306 Patent and attached a copy of Dr. Ryan's declaration and accompanying claim charts to his expert report. Peuto. Tr. at 1371-72; RX 616C. Exhibit B.

377. The "clarified function" column of the expert report for the Siann '306 Patent repeatedly states with particular elements of the Siann '306 patent that "a display memory controller including fetch and address logic is required but not disclosed." RX 616C. Exhibit B at S301948, S301950, S301953, S301955, S301960, S301963, S301967, S301969, S301980. For example, this comment appears twice on S3-01980, with respect to two elements of claim 1 of the Siann '306 Patent: the "first means for reading the stored graphics pixels at a first frequency," and the "second means for reading and storing the stored video pixels at a second frequency . . ." Id.; see also RX 4, Column 9, lines 55-59 (Siann '306 Patent).

378. Dr. Peuto testified at his deposition in this investigation that he agreed with the comment in the "clarified function" column of the claim charts for the Siann '306 Patent that "a display memory controller including fetch and address logic is required but not disclosed." Peuto, Tr. at 1376-77.

379. Dr. Peuto confirmed at the hearing that he stood by the comment in the "clarified function" column of the claim charts for the Siann '306 Patent that "a display memory controller including fetch and address logic is required but not disclosed." Peuto, Tr. at 1377-78. In particular, Dr. Peuto agreed that the specification of the Siann '306 Patent did not disclose a display memory controller including fetch and address logic. Peuto, Tr.

at 1378.

380. Dr. Peuto asserted that the claims of the Siann '306 Patent refer to a memory controller, but agreed that the patent did not disclose the specifics of such a memory controller. Peuto. Tr at 1378-79.

381. Dr. Peuto testified as follows:

> Q Did you find the page I was referring to, Dr. Peuto?
> A You mean 1980?
> Q Yes.
> A Yes, I do.
> Q Okay. And I've put up here on the overhead CDX-146, which is a blow-up of this page. The way we've received it, it's rather difficult to read. Do you see that at the top that says "claim chart for U.S. patent number 5,406,306"?
> A Yes, I do.
> Q Okay. And then the left-hand column it says "claims"?
> A Yes.
> Q And actually, that's just the first -- okay. And then there's a column that says "clarified function." Do you see that?
> A Yes.
> Q Did you work with Dr. Ryan on the clarified function column?
> A I was one of the participant in that work.
> Q You were involved with it?
> A I was involved with it.
> Q Okay. And do you see that under "first means," the second paragraph under clarified function, it says at the end of the sentence "display memory controller including fetch and address logic is required but not disclosed." Do you see that?
> A Where is that?
> Q It's -- if you look at the screen, the overhead projection, that may help you find it. It's basically the second paragraph under --
> A First mean?

Q Yes.

A I see that.

Q Okay. And then under "second means," at the end of the sentence, the same sentence appears, do you see that?

A I see that.

Q Now, that means that when you were working with Dr. Ryan on this you concluded that the Siann '306 patent required fetch and address logic but did not disclose it; is that correct?

A That's what it says.

Q And it was correct when this was written; correct?

A I wouldn't say that.

Q Were you involved in writing this?

A No -- excuse me. I was involved in writing it.

Q Do you recall that Mr. Jacobs took your deposition and asked you some questions about that precise passage?

A I do.

Q I'd like to ask you to turn to your deposition, which is tab 1.

A Tab 1.

Q And at page 109, line 4, there's a question concerning the Ryan report, and I'll skip down to column -- line 9 on page 109, and this is your answer. "I remember except for the fact that as an internal expert I reviewed everything we did and we discuss it together" --

A I'm sorry. Which line are you talking about?

Q Yes. I'm talking about page 109, line 9.

A Okay.

Q And the question actually preceding that is "what was that work," which is referring to your work with Dr. Ryan. Your answer is "I remember except for the fact, you know, as an internal expert, I reviewed everything we did and discuss it together. I participated in two major segments of his report, the analysis of the prior art and the claim chart drawing for the pixel 306 analysis."

And then if you move on to the bottom of page 109, there's an answer where you say "the work I participated in was in the clarified function. There is a column called "clarified function," and then in the column called "structural notes." Do you see that?

A Yes, I do.

Q And it's correct you worked on the clarified function column of the claim chart that we've just been

referring to; is that correct?

A This is correct.

Q That's attached to your expert report; correct?

A Yes.

Q All right. And then if we turn to page 113 -- actually, page 112, Mr. Jacobs refers -- addresses the column we've just been referring to, and at line 11, the question is "and then you see on the right side, it says 'graphic bus and fetching logic required but not disclosed'?

"Answer: Uh-huh.

"And the quote 'required but not disclosed' refers to the graphics bus and the fetching logic?

"Answer: The graphics bus, as shown is the fetching logic, that is required, but not disclosed."

Page 113, continuing, "question: And that was a conclusion with which you agreed when this report was put together; is that correct?

"Answer: That's correct."

And then the same question and answer is read for some other similar references elsewhere in the report, and skipping over to page 119 at line 3, the question is "and that was a conclusion with which you agreed when this report was prepared?"

A Excuse me.

Q Page 114.

A 114, yes.

Q Okay. Line 3, "question: And that was a conclusion with which you agreed when this report was prepared?

"Answer: That's correct.

"Question: And you spent a lot of time with the Siann '306 since then; correct?

"Answer: Since that time?

"Question. Yes.

"Answer: Or at that time?

"Question: Since then.

"Answer: Most of the time that I spent on '306 was at that time, not since then.

"Question: Okay. You're not going to testify at trial that you disagree with the analysis in Exhibit 5 that references the elements I just read to you; correct?

"Mr. Cordell: Object to form.

"The witness: I will not disagree with it."
Do you see that?
A Yes, I do.
Q Was that the testimony you gave?
A Correct.
Q Are you telling me now you disagree with your prior answer of the Siann '306 patent?
A No, I am not.
Q So you agree that in structure shown in the Siann '306 patent, that a display memory controller, including fetch and address logic is required but not disclosed; correct?
A Could you repeat what you just said?
Q Okay. Do you agree with me that in the Siann '306 patent, a display memory controller, including fetch and address logic, is required but not disclosed by the '306 patent?
A You use the word "patent." What do you mean by the word "patent"?
Q I mean the patent.
A So do you include the claims?
Q Well, what did you mean when you were talking in your expert report?
A I meant the whole patent, including the claims.
Q That's what I'm talking about.
A Well, it is not disclosed in the specification, but it is disclosed in the claims.
Q There's a reference to a memory controller; correct?
A That is correct.
Q But it does not disclose the specifics of that memory controller; correct?
A That's correct.

Peuto, Tr. at 1373-79.

382. With respect to the Siann '306 Patent's "first means for reading the stored graphics pixels" and "second means for reading and storing the stored video pixels", Dr. Peuto opined that "a display memory controller including fetch and address logic is required but not disclosed [in the specification]." RX 616C (Peuto report), Exhibit B at S3-01980.

2. The Bindlish '864 Patent

383. U.S. Patent No. 5,608,864 ("Bindlish '864 Patent) issued on March 4, 1997 from an application filed on April 29, 1994. RX 7.

384. The Bindlish '864 Patent is related to the Nordic Product. Bril, JX 2 at 110-15; Nally, Tr at 195.

385. Mr. Ferraro testified as follows:

> Q Isn't it true, Mr. Ferraro, that you believe that claim 37 is anticipated by the prior art of record in this case.
> A Yes, sir, that's true.
> Q And that's by the Bindlish reference; isn't that true?
> A Yes, sir, that's true.

Ferraro, Tr. at 1611.

386. Mr. Ferraro acknowledged that if the Bindlish '864 Patent were deemed prior art, it would anticipate Claim 37 of the '525 Patent. Ferraro, Tr. at 1611.

387. Cirrus acknowledges that if the Bindlish '864 Patent were deemed prior art, it would anticipate Claim 37 of the '525 Patent. Cirrus Post-Hearing Brief at 93, n.18.

388. Dr. Peuto testified as follows:

> Q Does the Bindlish '864 patent disclose the video port engineering? And I'd refer you to your claim chart, and I'll give you an opportunity to retract it, because I read that part of your claim chart which does refer to some parts of the patent, but I looked at them and they're about as far removed as I could possibly see from the video port.
> A Which claim chart are you talking about?
> Q I think this is your second supplemental report, which is tab 5.
> A My second?
> Q I'm sorry, your supplemental report. I think

you'll find it at page 46 actually. Actually, if you look at claim 13, which is page 48 and 49, when it talks about the port being to memory, it refers back to 6. So let's look at what it says here as to claim 6 of the Bindlish '864 patent.

A Yes.

Q Okay. And you refer to two places as supporting a video port for receiving real-time video data and circuitry for generating an address to said memory at which said real-time video data is stored, and I guess here you just refer above, so you have these two references which I guess you assert discloses a video port into memory; correct?

A Those references allude to such a port, yes.

Q Isn't it true that this first allusion is about as general as you could possibly be. It just says we are generally interested in things like playback and live video. This doesn't tell you anything about circuitry for generating addresses.

A I would agree.

Q Now, let's look at the second one. This does talk about a memory controller, but this is talking about data, graphics and video data from the CPU, and it talks about some other source via the host bus interface. Now, that's the first port in claim 13; isn't that right?

A Yes.

Q So this does not disclose a memory address generation circuitry for a second video port, does it?

A I would have to say yes.

Q Now, you agree that the Bindlish '864 patent does not talk about a color key in the sense of an 8-bit graphics word of data that is compared to a color key; correct?

A That's my understanding.

Peuto, Tr. at 1517-18.

389. The Bindlish '864 Patent states as follows: "Since the CRT address counter in memory controller 540 counts background memory cycles, during the VW display it may count an incorrect number corresponding to the VW pixel depth. To prevent such a wrong count, the CRT address counter may be stopped while the VW is displayed and loaded with a

value corresponding to the end of the VW and restart of the background display." Bindlish '864 Patent, Column 8, lines 51-57.

390. Dr. Peuto testified as follows:

> Q Okay. And is it your testimony today that the '864 Bindlish patent teaches that, during the display of VW data, you should continue to retrieve graphics data?
> A You say the patent teaches. That sounds to me like a legal word. So what do you mean?
> Q Discloses.
> A Not in a legal sense.
> Q Well, is there disclosure? Can you point me to disclosure in the '864 patent that indicates that graphics data is retrieved while VW data is displayed?
> A I interpret the figure 3 to provide some of that basis. Figure 3 is mentioned as 3A and 3B, so it's hard to find. It's a timing diagram.
> Q What does that tell you?
> A It tells me that the way the Bindlish patent makes reference to memory is it basically fills its FIFOs, and then at the bottom you see what you see on the screen, the VW being displayed.
> Q Yes.
> A And that I expect that where the dash lines are, you continue repeating the loading of the graphics FIFOs and the video FIFOs.

Peuto, Tr. at 1511-12.

391. Dr. Peuto subsequently testified as follows:

> Q And what I see here down at the bottom right-hand corner is there's a bracketed VW. Do you see that?
> A Yes.
> Q And when I look up, I don't see happening in the CRT FIFO, VW FIFO and CRT serializer; isn't that correct?
> A You're looking up into the dashed line.
> Q Are you saying the dash line means something?
> A Generally, yes.
> Q What does it mean?
> A In this context, it means gets repeated.

Q Meaning what?
A Meaning that the CRT FIFO that you saw, the CRT FIFO, which says 40 PELS, 60 PELS, will keep on being repeated.
Q And the CRT serializer is not a dashed line, it's a solid line; correct?
A Yes.
Q That means that graphics data is not going through the CRT serializer; correct?
A No, no place, it says the CRT serializer has graphic data going through it. This is a control circuit. Data goes through a path.
Q But it's a control circuit that relates to a particular part of the graphics pipeline; correct?
A I believe so.
Q And that circuitry is not active during the VW display period; correct?
A Yes.

Peuto, Tr. at 1514-15.

392. [ ] testimony, Tr. at 97-100, concerned the Nordic Product, and not specifically the Bindlish '864 Patent. [ ]

393. [ ] testimony regarding "always rastering" lacks clarity, and is unreliable. [ ]

394. The '525 Patent, in its entirety, does not suggest a distinction between "to" the pipeline and "through" the pipeline. CX 1.

395. The specification of the Bindlish '864 Patent includes a statement that "the data pipeline is kept full." RX 7, Column 10, line 38.

396. The specification of the Bindlish '864 Patent indicates that the CRT address counter may be stopped. RX 7, Column 8, lines 54-57.

E. <u>Section 102(g) – Invented by Others</u>

397. See previous findings of fact regarding Oak/Brooktree, *infra*.

F. Section 102(f) – Derivation of Invention

398. ATI withdrew this invalidity defense. ATI Post-Hearing Brief at 108.

G. Section 103

399. Mr. Ferraro opined that a person of ordinary skill in the art at the time of the '525 Patent "... would have been schooled in electrical engineering, would have two years of experience in digital circuitry design and would have sufficient systems knowledge so as to understand the block diagram of Figure 2 of the '525 Patent. Such a person would be versed in PC graphics, have some knowledge of video processing, but not necessarily have direct graphics or video controller chip design experience." CX 745C at 75 (Ferraro Rebuttal Report).

400. Mr. Ferraro opined:

> The overall contribution of an architecture lies in its unique design. In this respect, the value of the '525 patent is much greater than the sum of its individual parts. The interrelationship between circuit elements in an architecture determines its performance. One cannot necessarily add or subtract from a design without adversely affecting its performance. This is true for all architectural systems, the '525 and other prior art designs included. Dr. Peuto's implicit approach – searching for whether the individual elements were present in the prior art – if adopted, would invalidate virtually any patent on an architecture.
>
> CX 745C at 75 (Ferraro Rebuttal Report).

401. At the hearing, when questioned on cross-examination, ATI's expert, Dr. Peuto, was not prepared to give testimony regarding the teachings of the Romesburg '643 Patent. Peuto, Tr. at 1411-12.

402. Cirrus manufactured and sold the Cirrus Pixel CL-PX2070/CL-PX2080 and its upgrade,

the 2085 (collectively "2070/2080") prior to January 23, 1995. Schafer, Tr. at 640; RX 304; RX305.

403. Mr. Schafer testified as follows:

> Q And we're back to the 2070/2080. Isn't it true that the 2070/2080 products were sampled as a chip set around the fourth quarter of 1992?
> A That sounds right.
> Q And for the record, we're referring to RX-295. Isn't it true that the terms "sampling" within Cirrus includes delivery of chips to customers?
> A Yes.

Schafer, Tr. at 640.

404. The 2070/2080 consisted of several components that were designed and sold as a combination product. Schafer, Tr. at 628.

405. The 2070/2080 lacks a unified frame buffer, lacks the dual FIFOs described in Claims 16, 17, and 23, and does not perform vertical interpolation as set forth in Claim 23. ATI Post-Hearing Brief at 111-12.

406. The 2070/2080 had two separate frame buffers, one for graphics and one for video. Schafer, Tr. at 643; Ferraro, Tr. at 1571.

407. Mr. Nally testified that a unified frame buffer was desired by customers for cost savings and was a goal of the VESA Media Channel, an industry standards group. Nally, Tr. at 202, 204.

408. In his written expert report, Dr. Peuto stated in a conclusory fashion that implementation of a unified frame buffer for the two separate frame buffers in the 2070/2080 would have been obvious to one of skill in the art at the time of the '525 Patent invention. RX 618C

at 82.

409. Dr. Peuto offered no live testimony regarding the obviousness of substituting a unified frame buffer for the two separate frame buffers in the 2070/2080.

410. Mr. Ferraro testified as follows:

> Q And to come back to your obviousness discussion at the beginning, why wouldn't it have been obvious to compress those two separate frame buffers into a single frame buffer?
>
> A If you see the chain of events that led to the last row of my chart, all of that evolution of product had to take place to get from that dual frame buffer to the single frame buffer with the claim element. So it was not a simple -- it was not a simple thing to retrieve both graphics or video or to know how to do it and all that. So it's far from obvious.
>
> Q So you're pointing to sort of the great leap forward necessary to go from the pixel frame -- dual frame buffer approach to the '525 single frame buffer approach?
>
> A Yes.
>
> Q And that's sort of an empirical -- I guess that's an empirical basis for making an obvious determination, but from the technical engineering standpoint, why would it have been hard, with respect to the pixel products, to simply compress them into a single frame buffer?
>
> A Well, to have a single frame buffer, you'd have to have a single controller, and I don't think that they had the -- I don't think that it would have been obvious to someone picking up these two single controllers how to actually combine them and put it together. I mean, a lot of engineering would have been involved. And was involved.

Ferraro, Tr. at 1573-74.

411. Mr. Ferraro's expert testimony regarding the obviousness of substituting a unified frame buffer for two separate frame buffers is more credible and convincing than Dr. Peuto's expert testimony on this issue.

H. Section 112, ¶ 2

412. See Findings of Fact, *supra*, regarding indefiniteness of claim limitations.

I. Section 112, ¶ 1 - Written Description

413. ATI's pre-hearing brief failed to address this issue.

J. Section 112, ¶ 1 - Enablement

414. See Findings of Fact, *supra*, regarding indefiniteness of claim limitations.

K. Section 112, ¶ 1 - Best Mode

415. Mr. Nally testified as follows:

> Q I would like to get back to the FIFOs for a moment, if I can. You told me at your deposition that the small FIFOs were very important; correct?
> A Yes.
> Q And part of the reason why you said they were so important is that -- well, was that they were an advantage you realized by being able to grab small chunks of the data in each memory cycle; correct?
> A There was probably a miscommunication there. To grab small chunks of data. It allowed us to have a small FIFO.
> Q But the two are related; right?
> A Yes.
> Q So the small FIFO was the advantage you realized out of being able to grab the small chunks of data?
> A Yes.
> Q The idea in the '525 patent is that you don't have to go out and retrieve an entire line of data before displaying that line on the screen; correct?
> A A large portion -- you don't necessarily have to store the whole line but you've got to store a lot of data.
> Q But your chunk I, if we can call that, memory retrieval scheme allows you to get less than a full line? That is absolutely true isn't it?
> A Yes.
> Q That's a big advantage of the invention, isn't it?
> A Yes.

Q One of those advantages you pointed out is you don't need as big a FIFO; correct?

A Correct.

Q Now, doesn't that also mean that your FIFO has to continuously process data as each small chunk is fed into the input port of that FIFO?

A Only if the pipeline high-end FIFO is run.

Q I see. Good point. But in the case where the video pipeline is moving, is active, the video data is being displayed on the screen, that small FIFO needs to keep moving data through it at all times; correct?

A That is correct.

Q The FIFO will be emanating from the video -- strike that.

The video data will be emanating from the FIFO at at least the rate that it's being displayed on the CRT; correct?

A Not necessarily.

Q That's because you may have scaling downstream in the FIFO?

A Yeah. If you've got scaling going on, the rate of data coming out of FIFO does not match the rate of data going to the display screen.

Q Thought about it as soon as it left my mouth. You're exactly right. There may be the case where there's scaling. Let's take the case where there's no scaling, and that does happen?

A Right.

Q In the case where there's no scaling, the data is leaving the FIFO at [sic] at least the display rate of the CRT?

A Correct.

Q And that means that data has to be placed into the FIFO at at least that same rate; correct?

A That's correct.

Q So you continuously feed the small FIFO and continuously throw data out as long as the video pipeline is there?

A The difference is the back end is a steady stream. The front end is a chunkier, a burst scheme.

Q So we've got a bursting retrieval out of the memory into the small FIFO and the data is moving continuously through that FIFO and emanating at a regular rate?

A Correct.

Q And the interpolation scheme of the '525 patent takes data in word-sized units out of the FIFOs and then interpolates them word by word; correct?

A I believe so.

Q So the minimum burst of data that is retrieved in the '525 patent is a word data; correct?

A We treat the burst as a number of 32-bit increments. Okay? It might be four blocks of 32. It might be eight blocks of 32.

Q The idea is that it's some number -- some integral number of words that you're pulling out of memory with each burst; correct?

A Yes.

Q The idea behind the '525 patent, the thing that gives you these great advantages is you're able to take those bursts in very small chunks?

A Correct.

Nally, Tr. at 156-60.

416. Mr. Nally testified as follows:

Q Let's talk a little bit more about the small FIFO issue that we discussed back in your deposition. You thought that was a pretty good feature, didn't you?

A Yes, I did.

Q In fact, you characterized it as exciting; isn't that true?

A Yes.

Q But you didn't tell the Patent Office that this was an exciting feature, did you?

A I'm glad to say that what I thought I had to reveal to the Patent Office was what was unique and different, and what was really unique and different was the cycle stealing mechanism to allow me to have the small FIFOs. The small FIFOs was an achievement. It wasn't the -- what's the word I'm looking for here. It was the benefit of the real invention.

Q It was the advantage?

A It was the advantage. That's why I say it was the benefit of the invention. It gave me a real edge over my competitor.

Q You didn't tell the Patent Office this was the benefit of the invention, did you?

A No, I didn't think it had any bearing over the patent at all. I was supposed to disclose what the invention did, and I didn't think it was part of my job to do the marketing -- to say that -- engineering is engineering, marketing is marketing. I wear two hats. The marketing side of the architect saw an exciting feature. The engineering side of it saw something that had to be -- that was okay, this is something that I've got to explain to the Patent Office. What I'm doing. What I explained to the Patent Office is what I'm doing, and the marketing side is really excited because they're getting this feature and that feature is cycle stealing.

Q Earlier in your testimony today, I thought I heard you characterize a different feature as the key to the invention and that was the ability to put a video window on the screen under register control. Do you recall that?

A Yes.

Q Did you mean to say that that was a key to the invention?

A There's a number of key -- this is a system of architect, okay. A lot of things we did were key. If either one of these things was missing, we were going to probably be in the same boat as everybody else in the industry. We would have probably had a product that was almost good enough. So yeah, all these things to me were key, and every one of them had to be there.

Q Well, and you also said that you didn't see this in the prior art, this ability to position a video window under register control; isn't that right?

A Yeah, because everything I knew existed at the time was using mask tags.

Q And you also said that you were unaware of anyone else in the prior art providing for Y interpolations; isn't that true?

A That is true.

Nally, Tr. at 136-39.

IV. Enforceability

417. On May 2, 1995, the applicants filed a first Information Disclosure Statement identifying

the following eight prior art patents, all of which were cited earlier during the prosecution of a co-pending application (No. 08/098/846) that was incorporated by reference in the '525 Patent application: 5,257,348 (Roskowski *et al.*), 5,274,753 (Roskowski *et al.*), 5,229,852 (Maietta et al.), 5,341,318 (Balkanski et al.), 4,991,122 (Sanders), 5,365,278 (Willis), 5,341,442 (Barrett), and 5,218,432 (Wakeland). CX 2 at 143-47.

418. On January 17, 1996, the examiner issued a first Office Action rejecting the claims of the '525 patent application on the grounds that the claims were obvious in light of one or more of the following articles: (1) EDGE: Work-Group Computing Report, October 3, 1994, v5; (2) Jeff Mace "Mainstream Graphics Accelerators Rush Power," PC Magazine, Dec. 1994, v13; (3) Anthony Cataldo "WD, Cirrus Show Video Playback ICs," Electronic News, Oct. 1994, v40; and (4) Dave Bursky "Acceleration Puts the "Snap" into Graphics," Electronic Design, July 1994, v42. CX 2 at 151-59.

419. The examiner did not mention any particular products in the first Office Action. CX 2 at 151-59.

420. The articles the examiner cited report on the features of numerous products, including the Cirrus CL-GD5440 and CL-GD7542 products. CX 2; CX 26; CX 27; CX 28; CX 29.

421. Mr. Nally and Mr. Schafer designed the CL-GD5440 product. Schafer, Tr. 569.

422. The applicants responded to the first Office Action in their remarks following the Amendment Transmittal dated February 5, 1996, and in the supporting declarations of Mr. Nally and Mr. Schafer. CX 2 at 165-77

423. On February 5, 1996, the applicants submitted a second Information Disclosure Statement identifying U.S. Patent No. 5,406,306, the Siann '306 Patent. CX 2 at 161-63.

424. The second Information Disclosure Statement included the following statement

> The '306 patent is directed to the same general problem as is the invention disclosed in the above-identified patent application but deals with the problem in a different manner. In the '306 patent there is also a single memory for storing both graphics and video data. However, in the '306 patent the data is divided according to graphics or video with each being stored in a different portion of the memory. The data is then treated separately throughout the circuit. For example, the video data is processed at one frequency and the graphics data is processed at a different frequency. It is only when the two different data forms are actually sent to the monitor are they both processed at the same frequency. The '306 specification primarily deals with the concept of handling the processing of the different data forms (video and graphic) using different frequencies and does not, in any manner, deal with or even hint at the concept of dividing the data into on-screen and off-screen portions. Neither does the '306 patent deal with or even hint at 1) dividing the single memory into on-screen and off-screen portions, or 2) providing the on-screen and off-screen portions to the screen under control of different pipelines, as is specifically claimed in the invention in the above-identified application.

CX 2 at 162 (emphasis in original).

425. Mr. Nally testified that when he analyzed the Siann '306 Patent during the prosecution of the '525 Patent, he believed that the dotted line in Figure 3 of the Siann '306 Patent indicated that the Siann '306 Patent uses a split frame buffer, that is, a frame buffer in which half of the frame buffer is used for video and half is used for graphics. Nally, Tr. 106.

426. Mr. Nally testified that during the prosecution of the '525 Patent, he believed that the Siann '306 Patent involved a hard partition between video and graphics in its frame buffer, similar to schemes in which video data and graphics data were stored in entirely separate frame buffers. Nally, Tr. 107.

427. The text of the Siann '306 Patent does not contain the phrases "on-screen" or "off-screen." CX 157; Peuto, Tr. 1299.

428. Mr. Schafer's current understanding of the specification of the Siann '306 Patent is that it does suggest dividing a single frame buffer into on-screen and off-screen portions. Schafer, Tr. 631-32.

429. Mr. Nally now believes that part of the Siann '306 Patent specification describes dividing video and graphics data in a single frame buffer such that it could be interpreted as describing a memory having on-screen and off-screen areas. Nally, Tr. 214.

430. The concept of on-screen and off-screen memory is distinct from the concept of dividing memory into video and graphics portions. Ferraro, Tr. 504-08.

431. The examiner had the Siann '306 Patent before him when he evaluated the second Information Disclosure Statement, and for the remainder of the prosecution of the '525 Patent. CX 2 at 161-64.

432. In the first Office Action mailed January 17, 1996, the examiner referred to the concepts of on-screen and off-screen memory, even where those exact phrases had not been used, because he stated: "EDGE discloses that Cirrus Logic's MotionVideo Architecture includes a multi-format buffer that stores YUV signals from a video stream and RGB format from a computer (pg. 1). EDGE does not expressly disclose writing data to on-screen and off-screen memory of the frame buffer. However on-screen and off-screen memories are well known and common in the art and Mace teaches using off-screen memory to change resolution and color depth of the video." CX 2 at 153.

433. The Siann '306 Patent is one of the closest prior art references that has been presented in

the case. CX 745C at 78-79 (Ferraro Rebuttal Report).

434. Mr. Nally testified that he believes, and believed during the prosecution of the '525 Patent, that he was not required to disclose the Siann '306 Patent to the Patent Office because he believed that the Siann '306 Patent, being a two- or three-chip solution instead of the one-chip solution of the '525 Patent, was not significant prior art. Nally, Tr. 184.

435. [

]

436. [

]

437. [

]

438. [

]

439. Mr. Siann indicated that the Brooktree Bt885 "implemented some [but not all] of the particular circuitry as defined by the ['306] patent," and Mr. Ferraro therefore opined that it is therefore a cumulative reference because the applicants disclosed the Siann '306 Patent. CX 745C at 79 (Ferraro Rebuttal Report); see also Siann, Tr. 1041-42.

440. Mr. Nally testified that he believed, during the prosecution of the '525 Patent, that the 2070/2080 was not significant prior art because it is a two- or three-chip solution, not the one-chip solution of the '525 Patent. Nally, Tr. 184.

441. Mr. Nally and Mr. Schafer did not disclose the CL-GD5430 because it was a graphics-only device, and they believed it was not relevant to the '525 Patent. Schafer, Tr. 599-600

442. Mr. Nally testified that he did not disclose the Intel i750/DVI because he did not believe (and does not believe) that it is related to the '525 Patent. Nally, Tr. 184-85.

443. During the prosecution of the '525 Patent, Mr. Schafer had heard of the Intel i750 product, but did not know about its functionality, and does not recall reviewing any detailed specification of that product. Schafer, Tr. 597.

444. Mr. Nally testified that he believed, during the prosecution of the '525 Patent, that he was not required to disclose the 2070/2080 to the Patent Office because it was not significant to the '525 Patent. Nally, Tr. 184.

445. Mr. Nally testified that he believed, during the prosecution of the '525 Patent, that the Nordic product and the Bindlish '864 Patent were directed toward a technique for compressing video, and did not have anything to do with the '525 Patent. Nally, Tr. at 112-13.

446. Mr. Schafer testified that he did not disclose the Nordic product to the Patent Office because "the only features [he] was aware of on Nordic that were unique were very flat panel specific, and [he] didn't feel that that applied to the '525" Patent. Mr. Schafer also thought that anything in the Nordic CL-GD7542 relevant to the '525 Patent was

something that the CL-GD5440 team provided to the Nordic team, and therefore was something that Mr. Nally and Mr. Schafer invented. Schafer. Tr. at 593

447. [

]

Conclusions of Law

1. All conclusions of law set forth in the opinion are incorporated herein by reference

2. The U.S. International Trade Commission has personal jurisdiction over the parties and subject matter jurisdiction over this investigation.

3. ATI has imported and sold the accused products, the ATI Rage Devices.

4. The evidence proffered by Cirrus fails to demonstrate satisfaction of the domestic industry requirement of Section 337.

5. The evidence of record demonstrates that Claims 13, 15, 16, 17, 23 and 37 of the '525 Patent are invalid.

6. Even assuming, *arguendo*, the validity of Claims 13, 15, 16, 17, 23 and 37 of the '525 Patent, the evidence of record does not demonstrate that the ATI Rage Devices infringe these claims.

7. There is no violation of Section 337 with respect to the ATI Rage Devices and the '525 Patent.

INITIAL DETERMINATION AND ORDER

Based on the foregoing opinion, findings of facts, conclusions of law, and the record as a whole, and having considered all pleadings and arguments as well as proposed findings of fact and conclusions of law, it is my Initial Determination ("ID") that no violation of Section 337 exists in the importation into the United States, sale for importation, or sale within the United States of certain video graphics display controllers and products containing same.

I hereby certify to the Commission this ID, together with the record of the hearing in this investigation consisting of the following:

I. The transcript of the prehearing conference held on September 16, 1998, and the transcript of the hearing held from January 21, 1999 to January 29, 1999.

II. The exhibits accepted into evidence in this investigation as listed in the attached exhibit lists, and

III. All orders entered in this investigation as well as all pleadings, briefs and other documents and things filed with the Secretary.

In accordance with 19 C.F.R. § 210.39(c), all confidential material under 19 C.F.R. § 210.5 is to be given *in camera* treatment.

The Secretary shall serve a public version of this ID upon all parties of record and the confidential version upon counsel who are signatories to the Protective Order (Order No. 1) issued in this investigation, and the Commission investigative attorney. To expedite service of the public version, counsel are hereby Ordered to serve on my office no later than May 10, 1999, a copy of this ID with those sections considered by the party to be confidential bracketed

in red.

Pursuant to 19 C.F.R. § 210.42(h), this ID shall become the determination of the Commission unless a party files a petition for review pursuant to § 210.43(a) or the Commission, pursuant to § 210.44, orders on its own motion a review of the ID or certain issues herein.

Debra Morriss
Administrative Law Judge

Issued:

Exhibit List of the Administrative Law Judge
Inv. No. 337-TA-412

Exhibit Number	Description of Exhibit
ALJ Ex. 1	Transcript, including demonstrative aids, of Tutorial Session held on January 7, 1999